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AF/2112

PATENT APPLICATION

ATTORNEY DOCKET NO. 10016664-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Eric R. DeLano

Confirmation No.: 8893

Application No.: 10/044,401

Examiner: Lee, Christopher

Filing Date: 01/11/2002

Group Art Unit: 2112

Title: CUSTOMIZED PORTS IN A CROSSBAR AND METHOD FOR TRANSMITTING DATA BETWEEN CUSTOMIZED PORTS AND SYSTEM AGENTS

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **April 18, 2005**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Number of pages:

Typed Name: **Roger D. Greer**

Signature: Roger D. Greer

Respectfully submitted,

Eric R. DeLano

By Roger D. Greer

Roger D. Greer

Attorney/Agent for Applicant(s)
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Date: **June 20, 2005**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Eric DeLano
Serial No. 10/044,401
Filed: January 11, 2002
For: CUSTOMIZED PORTS IN A CROSSBAR AND METHOD FOR TRANSMITTING DATA BETWEEN CUSTOMIZED PORTS AND SYSTEM AGENTS
Group Art Unit: 2112
Confirmation No. 8893
Examiner: Lee, Christopher E.

I hereby certify that this paper is being deposited with the United States Postal Service as FIRST-CLASS mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this date.

6/20/05 *Date* *Registration No.* 26174

F-CLASS.WCM

Appr. February 20, 1998 *Attorney for Applicant*

APPELLANT'S BRIEF ON APPEAL PURSUANT TO RULE 192

REAL PARTY IN INTEREST

Hewlett-Packard Development Company.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims that are pending, finally rejected and appealed are 1-8, 10-14, 16 and 17. Claims 9 and 15 have been cancelled.

STATUS OF AMENDMENTS AFTER FINAL

No amendments were filed after the final office action dated January 18, 2005.

SUMMARY OF INVENTION

The invention concerns customized ports in a crossbar, which by way of background, is a chip or chip component commonly used to provide a processing system of high frequency links between multiple ports and system agents. In the prior art, each port has been generally designed as an input port for receiving data from system agents (i.e., source agents) and an output port for transmitting data from the input ports to other system agents (i.e., destination agents). The system agents can include multiple computer components, such as a central processing unit (CPU), Input/Output (I/O) controllers, memory controllers and cache memory.

The present invention provides a crossbar (Fig. 2, item 50) for providing connections between a plurality of ports (52, 54, 56, 58) and a plurality of system agents via a processing system (Fig. 3, 100), which includes a plurality of ports, with each port being capable of being an input port customized for receiving data from a source agent and an output port customized for transferring data to a destination agent, and crossbar control data (Page 6, para. 0019) for specifying crossbar control information for transferring data from an input port to an output port having different port configurations. (Pages 8-9, paras. 0023-0025)

The present invention also provides a method for transmitting data between customized ports and a plurality of system agents in a processing system (Fig. 3, 100) via a crossbar, which includes the steps of receiving data on an input port, obtaining the destination output port for the data received on the input port, determining whether the input port has the same configurations as the output port, obtaining control information from the crossbar control data when the input port does not have the same configurations as the output port, processing the data according to the obtained control information from the crossbar control data, and transmitting the

processed data to the destination output port. (Figs. 4 & 5, Pages 10-12, paras. 0027-0030)

ISSUES ON APPEAL

1. Whether the §112, second paragraph rejection of claims 12, 16 and 17 should be reversed because of applicant's use of the recitation "the width of the input port" and "the width of the output port", rather than the examiners' suggested recitations "a width of the input port" and "a width of the output port"?

2. Whether the §102(b) rejection of claims 1, 3, 6-8 and 11-13 based on Yokoyama (JP 411296473) should be reversed because of the examiner's misinterpretation of Yokoyama?

3. Whether the §103 rejection of claims 16 and 17 should be reversed as being based upon the misinterpretation of Yokoyama in combination with Lach?

GROUPING OF CLAIMS

To conduct this appeal economically and for the limited purposes of this appeal, dependent claims 2, 4, 5 and 10 stand or fall with associated independent claim 1; and dependent claims 13 and 14 stand or fall with associated independent claim 12.

ARGUMENT

1. The §112, Second Paragraph Rejection of Claims 12, 16 and 17 Should be Reversed Because of Applicant's use of the Recitation "the Width of the Input Port" and "the Width of the Output Port" is not indefinite.

Claims 12, 16 and 17 stand rejected under §112, second paragraph because of applicant's use of the recitation "the width of the input port" and "the width of the output port". The examiner maintained this rejection after applicant

declined the examiner's suggested use of the recitations "a width of the input port" and "a width of the output port". Applicant declined to make this change for the reason that the proposed change is simply awkward and unnecessary. It elevates form over substance. The applicant's usage would not be indefinite to one of ordinary skill in the art. Antecedent basis is not or should not be an issue with regard to *width* of a port, as every port has some width, particularly so in the context of these claims. However, applicant states that should this rejection be the sole impediment to an allowance of these claims, applicant consents to the examiner's proposed language change.

2. Claims 1, 3, 6-8 and 11-13 are not Anticipated Under §102(b) by Yokoyama When Yokoyama is Properly Interpreted.

Claims 1, 3, 6-8 and 11-13 stand rejected under §102 based on Yokoyama. This rejection should be reversed as it is based upon a misinterpretation of Yokoyama.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). "The ordinary and customary meaning of a claim term to one of ordinary skill in the art may be ascertained from a variety of sources, first, as *Vitronics* instructs, from the intrinsic evidence of record such as the claims themselves, the written description, and the prosecution history, but also from the 'common understanding' of the terms that may be reflected in dictionaries, encyclopedias, and treatises." *W.E. Hall Co., Inc. v. Atlanta Corrugating, LLC*, 370 F.3d 1343, 1350(Fed. Cir. 2004) (citation omitted). Claim terms are presumed to have the ordinary and customary meanings attributed to them by those of ordinary skill in the art. *Sunrace Roots Enter. Co. v. SRAM Corp.*, 336 F.3d 1298, 1302 (Fed. Cir. 2003). The broadest reasonable interpretation of the claims to be given during examination by the USPTO must be consistent with the interpretation that those skilled in the art would reach. *In re Cortright*, 165 F.3d 1353 (Fed. Cir. 1999).

With regard to the examiner's rejections, it is noted that the undersigned had a telephone interview with the examiner on September 1, 2004, in which the principal reference of Yokoyama was discussed. The undersigned stated that the extensive discussion of Yokoyama indicated that the examiner understood the Japanese language and that the comments that were made concerning this reference revealed considerable more knowledge than was set forth in the abstract that was provided by the EPO which consisted of less than a full page of description relating to the nature of the operation of the Yokoyama system.

The examiner indicated that he did read Japanese and also informed applicant that the Japanese Patent Office had a free computer translation system in which an English translation could be obtained and offered to acquire and fax the English translation to applicant, which was done. The examiner indicated that such computerized translations are often inaccurate and difficult to understand. In the cover letter of the facsimile transmittal, the examiner specifically cautioned the applicant that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely. The translation itself contains similar language. It is also indicated that none of the text shown in the drawings are translated in this machine translation.

The undersigned wishes to point out that the translation was indeed difficult to understand and that the examiner has also relied on descriptions of text contained in drawings which applicant is unable to verify the accuracy of or at least fully consider. Applicant formally requested that if the amendments that are made herein were unsuccessful and if Yokoyama continued to be a basis for rejection of the claims of this application, an accurate translation from the USPTO should be provided to applicant. The USPTO did not supply any additional translation.

Because applicant believed that he was disadvantaged by the potential of an incorrect translation, a separate translation was ordered. The second translation was of little assistance. Both of the translations are enclosed with this brief for the possible consideration of the Board.

With regard to amended claim 1, the examiner's position with regard to Yokoyama anticipating the following element recitation:

> *crossbar control data for specifying crossbar control information for transferring data from an input port to an output port having different port configurations, said crossbar control data containing control information for* ***formatting*** *bit length of data from an input port to be transmitted to an output port* ***having less width than the input port,***

was that setting switches 2 and 3 make the port configure as an output port according to Figs. 3 and 11, with less width than said input port and cites Fig. 24 and paragraph 0149.

The examiner's reliance on Fig. 24 is not instructive as it merely shows a table of control numbers, i.e., C1 through C9, which essentially seems to show that a 256 bit band can be secured for transmitting 128 bit or 256 bit data, with paragraph 0149 reading "C6 shows the case where 128 bit band can be secured in case 256 bit data are transmitted to a 128 bit port and in case C7 transmits 256 bit data to 128 bit port, it shows the case where a band is not securable." Nowhere else in the specification, to the extent that applicant can understand it, is there any discussion that data is **formatted** at all.

All of the other cases (C1-C5 and C8-C9) indicate that data is either smaller or the same size as the output port capacity, and if not, the band is not securable. There is no discussion why or how case C6 differs from case C7 anywhere in the 25 page translation. It is submitted that the described case C6 is either gratuitous or erroneous. Nowhere in the specification does it indicate that data is reformatted to fit the width of the output port if the output port capacity is less than that of the input port.

Claim 11 is also believed to be allowable for the reason that Yokoyama totally fails to anticipate, teach or suggest a crossbar having a plurality of virtual communication channels on each input port. The examiner attempts to equate a plurality of virtual communication channels on each input port to data paths that are

provided by the interconnection of switches in Fig. 5. Applicant believes that this is a totally misplaced reliance on the switch configuration shown in Fig. 5. It has nothing to do with virtual communication channels that are claimed.

Claim 12 is also believed to be allowable over Yokoyama essentially for the same reasons as set forth above with regard to claim 1.

3. Claims 16 and 17 are not Obvious Over Yokoyama in View of Lach

The examiner's position with regard to the amendatory language that was added to claims 16 and 17 (and to claim 12), namely:

> *wherein said step of processing the data further comprising the steps of:*
>
> *determining whether the width of the input port is more than the width of the output port;*
>
> *submitting the data as processed data when the width of the input port is not more than the width of the output port;*
>
> *obtaining the width of the output port when the width of the input port is greater than the width of the output port;*
>
> *formatting the data from the input port to data configured for the obtained width of the output port;*
>
> *submitting the formatted data as the processed data;*

was that Yokoyama meets the formatting step by Box S20 in Fig. 14, which is untranslated Japanese text that appears to be unimportant, and paragraphs 0090-0091. Paragraphs 0090-0091 in the computer-generated translation read as follows:

> "[0090] A discernment bit secures the near path of '1' and the crossbar switch side address control section 61-1 relays a transfer OK signal to the address control section 81-1 in a

board of the processor board 2-1 (drawing 14 step S20). [0091] In this case, the crossbar switch side address control section 61-1 records the path and phase hand information which were secured to (memory B) 61C-1 (drawing 14 step S20). Henceforth, with reference to the path and phase hand information which were recorded on (memory B) 61C-1, it checks about the signal from the address control section 81-1 in a board, and if it is a signal from the same communications partner, the junction of the signal will be continued till transfer termination (drawing 14 step S21). In addition, if the crossbar switch side address control section 61-1 becomes transfer termination, it will eliminate the path information on (memory B) 61C-1 simultaneously (drawing 14 step S22)."

Clearly, these paragraphs cited by the examiner have nothing to do with the step of processing the data which comprises the steps of determining whether the width of the input port is more than the width of the output port, submitting the data as processed data when the width of the input port is not more than the width of the output port, obtaining the width of the output port when the width of the input port is greater than the width of the output port; and formatting the data from the input port to data configured for the obtained width of the output port and submitted the formatted data as processed data. This is simply not done by Yokoyama. As can be best understood, Yokoyama transmits 128 bit data or 256 bit data through ports that are capable of handling the various sized data. The system attempts to secure a band for transmission which may or may not be successful. There is no discussion that has been located which indicates that data is **reformatted** so that it is configured for the obtained width of the output port.

The examiner cites col. 12, lines 3-9 of Lach for the proposition that he takes Official Notice that flow steps can be implemented with the "same or equivalent results" and is well know to those of ordinary skill in the art: *Further, various techniques of the invention may be achieved in either all software implementations,*

using appropriate processor instructions, or in all hardware logic implementations, or in hybrid implementations that utilize a combination of hardware logic and software logic to achieve the same or equivalent results.

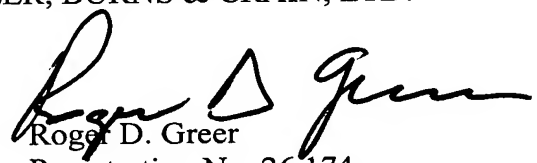
The examiner ignores the fact that Yokoyama fails to teach or suggest the flow steps themselves and Lach simply fails to supply the basic deficiency of Yokoyama. The examiner's Official Notice does not help him.

CONCLUSION

For the above reasons, Applicant requests the Board to reverse the outstanding rejections. The case should then be permitted to pass to allowance.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

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CLAIMS:

1. A crossbar for providing connections between a plurality of ports and a plurality of system agents via a processing system comprising:

a plurality of ports, each port capable of being an input port customized for receiving data from a source agent and an output port customized for transferring data to a destination agent; and,

crossbar control data for specifying crossbar control information for transferring data from an input port to an output port having different port configurations, said crossbar control data containing control information for formatting bit length of data from an input port to be transmitted to an output port having less width than the input port.

2. The crossbar according to claim 1 wherein the data received on the input port further comprises control data for indicating validity and destination information relating to data received on the input port.

3. The crossbar according to claim 1 further comprising at least one register on each input port and each said output port for storing data in memory.

4. The crossbar according to claim 1 further comprising at least one shift register on each input port for storing data in memory and shifting data with larger bit length to a smaller bit length data for transmission from an input port with more width to an output port with less width.

5. The crossbar according to claim 1 further comprising at least one multiplexor device on each said input port and each said output port for prioritizing transmissions of data.

6. The crossbar according to claim 1 wherein an input port and an output port of at least one of said plurality of ports are customized to have different widths.

7. The crossbar according to claim 1 wherein a plurality of said input ports are customized to have different width.

8. The crossbar according to claim 1 wherein a plurality of said output ports are customized to have different width.

9. Cancelled.

10. The crossbar according to claim 1 wherein said crossbar control data contain control information for use by any one from the group of a shift register or a multiplexor device.

11. A crossbar having a plurality of paths for providing connections between a plurality of ports and a plurality of system agents via a processing system comprising:

a plurality of ports, each port capable of being an input port customized for receiving data from a source agent and an output port customized for transferring data to a destination agent;

a plurality of virtual communication channels on each input port; and,

crossbar control data for specifying crossbar control information for transferring data from a virtual communication channel to an output port having different configurations.

12. A method for transmitting data between customized ports and a plurality of system agents in a processing system via a crossbar, wherein the crossbar includes a plurality of ports, each port capable of being an input port customized for receiving data from a source agent and an output port customized for transferring data to a destination agent, and crossbar control data for specifying crossbar control information for transmitting data from an input port to an output port having different port configurations, the method comprising the steps of:

receiving data on an input port;

obtaining the destination output port for the data received on the input port;

determining whether the input port has the same configuration as the output port;

obtaining control information from the crossbar control data when the input port does not have the same configurations as the output port;

processing the data according to the obtained control information from the crossbar control data;

wherein said step of processing the data further comprising the steps of:

determining whether the width of the input port is more than the width of the output port;

submitting the data as processed data when the width of the input port is not more than the width of the output port;

obtaining the width of the output port when the width of the input port is greater than the width of the output port;

formatting the data from the input port to data configured for the obtained width of the output port;

submitting the formatted data as the processed data; and,

transmitting the processed data to a destination output port.

13. The method according to claim 12 wherein said step of receiving data further comprises the steps of:

reading control data received with the data on the input port;

determining whether the control data have valid port information; and,

aborting when the control data does not have valid port information.

14. The method according to claim 13 wherein said step of obtaining the destination output port further comprises the step of obtaining the destination output port from the control data when the control data has valid port information.

15. Cancelled.

16. A system for transmitting data between customized ports and a plurality of system agents in a processing system via a crossbar, wherein the crossbar includes a plurality of ports, each port capable of being an input port customized for receiving data from a source agent and an output port customized for transferring data to a destination agent, and crossbar control data for indicating crossbar control information for transmitting data from an input port to an output port having different port configurations, comprising:

a storage medium;

a machine for transmitting data between customized ports and a plurality of system agents in a processing system via a crossbar, the machine comprising a set of instructions for:

receiving data on an input port;

obtaining a destination output port for the data received on the input port;

determining whether the input port has the same configuration as the output port;

obtaining control information from the crossbar control data when the input port does not have the same configurations as the output port;

processing the data according to the obtained control information from the crossbar control data;

wherein said step of processing the data further comprising the steps of:

determining whether the width of the input port is more than the width of the output port;

submitting the data as processed data when the width of the input port is not more than the width of the output port;

obtaining the width of the output port when the width of the input port is greater than the width of the output port;

formatting the data from the input port to data configured for the obtained width of the output port;

submitting the formatted data as the processed data; and,

transmitting the processed data to the destination output port.

17. A machine for transmitting data between customized ports and a plurality of system agents in a processing system via a crossbar, the machine comprising a set of instructions to:

receive data on an input port;

obtain a destination output port for the data received on the input port;

determine whether the input port has the same configuration as the output port;

obtain control information from a crossbar control data when the input port does not have the same configurations as the output port;

process the data according to the obtained control information from the crossbar control data;

wherein the processing of the data further comprising:

determining whether the width of the input port is more than the width of the output port;

submitting the data as processed data when the width of the input port is not more than the width of the output port;

obtaining the width of the output port when the width of the input port is greater than the width of the output port;

formatting the data from the input port to data configured for the obtained width of the output port; and,

submitting the formatted data as the processed data; and,

transmit the processed data to the destination output port.

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	15/16			15/16	４００Ｂ
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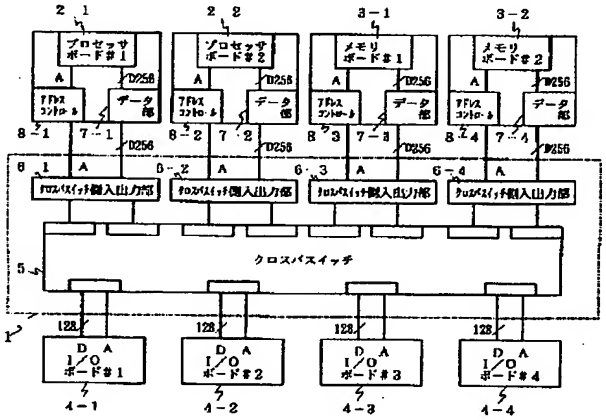
(54)【発明の名称】　データ幅可変型クロスバスイッチ装置及びその接続方法並びにその制御プログラムを記録した記録媒体

(57)【要約】

【課題】　クロスバスイッチに接続されたデータ幅が広いポートにおいて、データ幅が狭いポートとの通信中にも相手先のポートのデータ幅に関わらず通信可能なデータ幅可変型クロスバスイッチ装置を提供する。

【解決手段】　プロセッサボード２－１，２－２及びメモリボード３－１，３－２とクロスバスイッチ５との間に配置したクロスバスイッチ側入出力部６－１～６－４とデータ部７－１～７－４及びアドレスコントロール部８－１～８－４とによって、通信するボード同士のデータ幅が異なる際に、データ幅が広いポートを持つ側のボードの空いたポートで他のボードとの通信を行われる。データ部７－１～７－４で通信相手毎にデータを振り分け、振り分けたデータを２系統のバッファ群各々で保存する。アドレスコントロール部８－１～８－４は入出力データの経路をデータ部７－１～７－４に指示する。



【特許請求の範囲】

【請求項１】　複数のボードが夫々接続される同一データ幅の複数のポートを有し、前記複数のポートを介して前記複数のボード間を接続するデータ幅可変型クロスバスイッチ装置であって、通信するボード同士のデータ幅が異なる際に、前記データ幅が広いボードが接続されるポートのうちの空いているポートを介して他のボードとの通信を行うよう構成したことを特徴とするデータ幅可変型クロスバスイッチ装置。

【請求項２】　複数のボードが夫々接続される同一データ幅の複数のポートを有し、前記複数のポートを介して前記複数のボード間を接続するデータ幅可変型クロスバスイッチ装置であって、通信するボード同士のデータ幅が異なる際に前記データ幅が広いボードが接続されるポートのうちの空いているポートを検出する検出手段と、前記検出手段で検出したポートを介して他のボードとの通信を行う手段とを有することを特徴とするデータ幅可変型クロスバスイッチ装置。

【請求項３】　前記データ幅が広いボードに前記複数のポートを割り当てるよう構成したことを特徴とする請求項２記載のデータ幅可変型クロスバスイッチ装置。

【請求項４】　前記検出手段は、前記データ幅が広いボードに割り当てられた複数のポートの中から空いているポートを検出するよう構成したことを特徴とする請求項３記載のデータ幅可変型クロスバスイッチ装置。

【請求項５】　前記検出手段は、前記データ幅が広いボードに割り当てられた複数のポート各々からのアドレス情報を基に前記複数のポートのうちの使用中のポートを特定するよう構成したことを特徴とする請求項３または請求項４記載のデータ幅可変型クロスバスイッチ装置。

【請求項６】　前記検出手段は、前記複数のボード各々に割り当てられたポートの情報を記憶する記憶手段と、前記複数のボード各々に割り当てられたポート毎に通信相手のボード及び当該ボードに割り当てられたポート各々を特定する情報を保持する保持手段とを含むことを特徴とする請求項３から請求項５のいずれか記載のデータ幅可変型クロスバスイッチ装置。

【請求項７】　前記データ幅が広いボードのデータ幅を持ちかつ当該ボードと通信相手との間で授受されるデータを格納する第１及び第２の格納手段を当該ボードに含むことを特徴とする請求項２から請求項６のいずれか記載のデータ幅可変型クロスバスイッチ装置。

【請求項８】　前記データ幅が広いボードと通信相手との間で授受されるデータの入出力経路を設定する設定手段を当該ボードに含むことを特徴とする請求項２から請求項７のいずれか記載のデータ幅可変型クロスバスイッチ装置。

【請求項９】　複数のボードが夫々接続される同一データ幅の複数のポートを有し、前記複数のポートを介して前記複数のボード間を接続するデータ幅可変型クロスバスイッチ装置の接続方法であって、通信するボード同士のデータ幅が異なる際に、前記データ幅が広いボードが接続されるポートのうちの空いているポートを介して他のボードとの通信を行うようにしたことを特徴とするデータ幅可変型クロスバスイッチ装置の接続方法。

【請求項１０】　複数のボードが夫々接続される同一データ幅の複数のポートを有し、前記複数のポートを介して前記複数のボード間を接続するデータ幅可変型クロスバスイッチ装置の接続方法であって、通信するボード同士のデータ幅が異なる際に前記データ幅が広いボードが接続されるポートのうちの空いているポートを検出するステップと、その検出したポートを介して他のボードとの通信を行うステップとを有することを特徴とするデータ幅可変型クロスバスイッチ装置の接続方法。

【請求項１１】　前記データ幅が広いボードに前記複数のポートを割り当てるようにしたことを特徴とする請求項１０記載のデータ幅可変型クロスバスイッチ装置の接続方法。

【請求項１２】　前記空いているポートを検出するステップは、前記データ幅が広いボードに割り当てられた複数のポートの中から空いているポートを検出するよう構成したことを特徴とする請求項１１記載のデータ幅可変型クロスバスイッチ装置の接続方法。

【請求項１３】　前記空いているポートを検出するステップは、前記データ幅が広いボードに割り当てられた複数のポート各々からのアドレス情報を基に前記複数のポートのうちの使用中のポートを特定するようにしたことを特徴とする請求項１１または請求項１２記載のデータ幅可変型クロスバスイッチ装置の接続方法。

【請求項１４】　前記空いているポートを検出するステップは、前記複数のボード各々に割り当てられたポートの情報を記憶する記憶手段と、前記複数のボード各々に割り当てられたポート毎に通信相手のボード及び当該ボードに割り当てられたポート各々を特定する情報を保持する保持手段とを用いて前記空いているポートを検出するようにしたことを特徴とする請求項１１から請求項１３のいずれか記載のデータ幅可変型クロスバスイッチ装置の接続方法。

【請求項１５】　前記データ幅が広いボードのデータ幅を持つ第１及び第２の格納手段のうちの一方に当該ボードと通信相手との間で授受されるデータを格納するようにしたことを特徴とする請求項１１から請求項１４のいずれか記載のデータ幅可変型クロスバスイッチ装置の接続方法。

【請求項１６】　前記データ幅が広いボードと通信相手との間で授受されるデータの入出力経路を設定するステップを含むことを特徴とする請求項１０から請求項１５のいずれか記載のデータ幅可変型クロスバスイッチ装置の接続方法。

【請求項１７】　複数のボードが夫々接続される同一デ

ータ幅の複数のポートを有し、前記複数のポートを介して前記複数のボード間を接続する処理をプロセッサに行わせるための接続制御プログラムを記録した記録媒体であって、前記接続制御プログラムは前記プロセッサに、通信するボード同士のデータ幅が異なる際に、前記データ幅が広いボードが接続されるポートのうちの空いているポートを介して他のボードとの通信を行わせることを特徴とする接続制御プログラムを記録した記録媒体。

【請求項１８】　複数のボードが夫々接続される同一データ幅の複数のポートを有し、前記複数のポートを介して前記複数のボード間を接続する処理をプロセッサに行わせるための接続制御プログラムを記録した記録媒体であって、前記接続制御プログラムは前記プロセッサに、通信するボード同士のデータ幅が異なる際に前記データ幅が広いボードが接続されるポートのうちの空いているポートを検出させ、その検出したポートを介して他のボードとの通信を行わせることを特徴とする接続制御プログラムを記録した記録媒体。

【請求項１９】　前記接続制御プログラムは前記プロセッサに、前記空いているポートを検出させる際に、前記データ幅が広いボードに割り当てられた複数のポートの中から空いているポートを検出させることを特徴とする請求項１８記載の接続制御プログラムを記録した記録媒体。

【請求項２０】　前記接続制御プログラムは前記プロセッサに、前記空いているポートを検出させる際に、前記データ幅が広いボードに割り当てられた複数のポート各々からのアドレス情報を基に前記複数のポートのうちの使用中のポートを特定させることを特徴とする請求項１８または請求項１９記載の接続制御プログラムを記録した記録媒体。

【請求項２１】　前記接続制御プログラムは前記プロセッサに、前記空いているポートを検出させる際に、前記複数のボード各々に割り当てられたポートの情報を記憶する記憶手段と、前記複数のボード各々に割り当てられたポート毎に通信相手のボード及び当該ボードに割り当てられたポート各々を特定する情報を保持する保持手段とを用いて前記空いているポートを検出させることを特徴とする請求項１８から請求項２０のいずれか記載の接続制御プログラムを記録した記録媒体。

【請求項２２】　前記接続制御プログラムは前記プロセッサに、前記データ幅が広いボードのデータ幅を持つ第１及び第２の格納手段のうちの一方に当該ボードと通信相手との間で授受されるデータを格納させることを特徴とする請求項１８から請求項２１のいずれか記載の接続制御プログラムを記録した記録媒体。

【請求項２３】　前記接続制御プログラムは前記プロセッサに、前記データ幅が広いボードと通信相手との間で授受されるデータの入出力経路を設定させることを特徴とする請求項１８から請求項２２のいずれか記載の接続制御プログラムを記録した記録媒体。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はデータ幅可変型クロスバスイッチ装置及びその接続方法並びにその制御プログラムを記録した記録媒体に関し、特に異なるデータ幅を持つポート間を接続するクロスバスイッチ装置に関する。

【０００２】

【従来の技術】従来、この種のクロスバスイッチ装置においては、図３９に示すように、プロセッサボード（＃１～＃３）２－１～２－３とメモリボード（＃１～＃３）３－１～３－３とＩ／Ｏ（入出力）ボード（＃１～＃６）４－１～４－６とをクロスバスイッチ５を介して相互に接続している。

【０００３】この場合、プロセッサボード（＃１～＃３）２－１～２－３とメモリボード（＃１～＃３）３－１～３－３とＩ／Ｏ（入出力）ボード（＃１～＃６）４－１～４－６とは夫々異なるデータ幅を有している。つまり、クロスバスイッチ５は異なるデータ幅のポート間を接続している。

【０００４】ここで、プロセッサボード（＃１）２－１には、図４０に示すように、プロセッサ２１－１と、コントローラ２２－１と、入力バッファ２３－１と、出力バッファ２４－１とが搭載されており、それらがボード内バス２００－１で相互に接続されている。

【０００５】尚、図示していないが、他のプロセッサボード（＃２，＃３）２－２，２－３も上記のプロセッサボード（＃１）２－１と同様の構成となっている。また、上記と同様に図示していないが、メモリボード（＃１～＃３）３－１～３－３やＩ／Ｏ（入出力）ボード（＃１～＃６）４－１～４－６もプロセッサ２１－１の代わりにメモリやＩ／Ｏを搭載する以外は上記のプロセッサボード（＃１）２－１と同様の構成となっている。

【０００６】上記のクロスバスイッチ装置では、コントローラ２２－１が入力バッファ２３－１と出力バッファ２４－１とを制御することで、同じデータ幅のポート同士での通信を行っている。

【０００７】

【発明が解決しようとする課題】上述した従来のクロスバスイッチ装置では、クロスバスイッチが異なるデータ幅のポート間を接続しているが、異なるデータ幅の間をクロスバスイッチで接続すると、データ幅が狭いポートとの間で通信しているとデータ幅が広いポートとの間での転送ができない。

【０００８】また、メモリ等一部の同時アクセス要求の可能性が高い部分について、別にデータ幅の広い転送経路を用意することによって上記の問題を解決することができるが、その場合には使用効率が低くなり、ハードウェア量の増加を招いてしまう。

【０００９】さらに、データ幅が広いポートの代わりに複数のデータ幅が狭いポートを複数同一ボード上に持たせることで上記の課題を解決することもできるが、該当ボードとクロスバスイッチとを接続するアドレス線やコントローラも複数必要となり、ハードウェア量の大幅な増大を招いてしまう。

【００１０】そこで、本発明の目的は上記の問題点を解消し、クロスバスイッチに接続されたデータ幅が広いポートにおいて、データ幅が狭いポートとの通信中にも相手先のポートのデータ幅に関わらず通信することができるデータ幅可変型クロスバスイッチ装置及びその接続方法並びにその制御プログラムを記録した記録媒体を提供することにある。

【００１１】

【課題を解決するための手段】本発明によるデータ幅可変型クロスバスイッチ装置は、複数のボードが夫々接続される同一データ幅の複数のポートを有し、前記複数のポートを介して前記複数のボード間を接続するデータ幅可変型クロスバスイッチ装置であって、通信するボード同士のデータ幅が異なる際に、データ幅が広いボードが接続されるポートのうちの空いているポートを介して他のボードとの通信を行うよう構成している。

【００１２】本発明による他のデータ幅可変型クロスバスイッチ装置は、複数のボードが夫々接続される同一データ幅の複数のポートを有し、前記複数のポートを介して前記複数のボード間を接続するデータ幅可変型クロスバスイッチ装置であって、通信するボード同士のデータ幅が異なる際にデータ幅が広いボードが接続されるポートのうちの空いているポートを検出する検出手段と、前記検出手段で検出したポートを介して他のボードとの通信を行う手段とを備えている。

【００１３】本発明によるデータ幅可変型クロスバスイッチ装置の接続方法は、複数のボードが夫々接続される同一データ幅の複数のポートを有し、前記複数のポートを介して前記複数のボード間を接続するデータ幅可変型クロスバスイッチ装置の接続方法であって、通信するボード同士のデータ幅が異なる際に、データ幅が広いボードが接続されるポートのうちの空いているポートを介して他のボードとの通信を行うようにしている。

【００１４】本発明による他のデータ幅可変型クロスバスイッチ装置の接続方法は、複数のボードが夫々接続される同一データ幅の複数のポートを有し、前記複数のポートを介して前記複数のボード間を接続するデータ幅可変型クロスバスイッチ装置の接続方法であって、通信するボード同士のデータ幅が異なる際にデータ幅が広いボードが接続されるポートのうちの空いているポートを検出するステップと、その検出したポートを介して他のボードとの通信を行うステップとを備えている。

【００１５】本発明による接続制御プログラムを記録した記録媒体は、複数のボードが夫々接続される同一データ幅の複数のポートを有し、前記複数のポートを介して前記複数のボード間を接続する処理をプロセッサに行わせるための接続制御プログラムを記録した記録媒体であって、前記接続制御プログラムは前記プロセッサに、通信するボード同士のデータ幅が異なる際に、データ幅が広いボードが接続されるポートのうちの空いているポートを介して他のボードとの通信を行わせている。

【００１６】本発明による他の接続制御プログラムを記録した記録媒体は、複数のボードが夫々接続される同一データ幅の複数のポートを有し、前記複数のポートを介して前記複数のボード間を接続する処理をプロセッサに行わせるための接続制御プログラムを記録した記録媒体であって、前記接続制御プログラムは前記プロセッサに、通信するボード同士のデータ幅が異なる際にデータ幅が広いボードが接続されるポートのうちの空いているポートを検出させ、その検出したポートを介して他のボードとの通信を行わせている。

【００１７】すなわち、本発明のデータ幅可変型クロスバスイッチ装置は、通信するボード同士のデータ幅が異なる際に、データ幅が広いポートを持つ側のボードの空いたポートで他のボードとの通信ができるようにしている。

【００１８】すなわち、ボード内スイッチを設け、通信相手毎にデータを振り分ける。また、データ部にはボード内スイッチに加えて、データ幅が広いポートの最大データ幅と同じデータ幅を持つバッファ群を２系統設け、ボード内スイッチで振り分けられたデータを各々保存している。ボード内スイッチ制御部はボード内アドレス制御部からの信号に基づいて入出力データの経路をボード内スイッチに設けられた各スイッチ（ＳＷ）に指示する。

【００１９】上記のように、２系統のデータを保存する仕組みと、データを振り分ける制御機構とを持つことによって、データ幅が広いポートを持つボード内のクロスバスイッチへのポートを分割使用することが可能となる。

【００２０】

【発明の実施の形態】次に、本発明の一実施例について図面を参照して説明する。図１は本発明の一実施例によるクロスバスイッチ装置の構成を示すブロック図である。図において、クロスバスイッチ装置１はクロスバスイッチ５と、クロスバスイッチ側入出力部６－１～６－４とを備え、データ幅の広いプロセッサボード（＃１，＃２）２－１，２－２及びメモリボード（＃１，＃２）３－１，３－２各々に対応してデータ部７－１～７－４及びアドレスコントロール部８－１～８－４が配設されている。

【００２１】クロスバスイッチ５は１２８ビットのポートを１２個持ち、データ幅が１２８ビット幅のＩ／Ｏ（入出力）ボード（＃１～＃４）４－１～４－４を１２

８ビットのポートにそのまま接続し、データ幅が２５６ビット幅のプロセッサボード２－１，２－２及びメモリボード３－１，３－２を１２８ビットのポート２個に夫々接続している。

【００２２】すなわち、クロスバスイッチ装置１はプロセッサボード２－１，２－２及びメモリボード３－１，３－２を、クロスバスイッチ５の２つのポートに接続されたクロスバスイッチ側入出力部６－１～６－４を介して接続している。

【００２３】上記のクロスバスイッチ側入出力部６－１～６－４とデータ部７－１～７－４とアドレスコントロール部８－１～８－４とによって、通信するボード同士のデータ幅が異なる際に（例えば、プロセッサボード２－１，２－２及びメモリボード３－１，３－２はＩ／Ｏボード（＃１～＃４）４－１～４－４よりもデータ幅が大きい）、データ幅が広いポートを持つ側のボードの空いたポートで他のボードとの通信ができるようにしている。

【００２４】つまり、データ部７－１～７－４にボード内スイッチ（図示せず）を設け、通信相手毎にデータを振り分ける。また、データ部７－１～７－４にはボード内スイッチに加えて２５６ビット幅のバッファ群（図示せず）を２系統設け、ボード内スイッチで振り分けられたデータを２系統のバッファ群各々で保存している。

【００２５】アドレスコントロール部８－１～８－４に設けたボード内スイッチ制御部（図示せず）はボード内アドレス制御部（図示せず）からの信号に基づいて入出力データの経路をボード内スイッチに設けられた各スイッチ（ＳＷ）に指示する。

【００２６】上記のように、２系統のデータを保存する仕組みと、データを振り分ける制御機構とを持つことによって、データ幅が広いポートを持つボード内のクロスバスイッチ５へのポートを分割使用することが可能となる。

【００２７】尚、本発明の一実施例ではクロスバスイッチ装置１をアドレス／データ分離型とし、アドレス線を使用しかつ予め決められた信号によって通信経路の確保と、転送開始や転送終了等とを行い、適切なデータを入出力可能な仕組みを実現している。

【００２８】図２は図１のクロスバスイッチ側入出力部６－１の構成を示すブロック図である。図において、クロスバスイッチ側入出力部６－１はクロスバスイッチ側アドレス制御部６１－１を備えている。

【００２９】クロスバスイッチ側入出力部６－１はクロスバスイッチ５の２つのポートにアドレス線（Ａ）及び１２８ビットのデータ線（Ｄ）で接続され、プロセッサボード２－１にアドレス線（Ａ）と識別ビット（ｂｉｔ）（Ｓａ，Ｓｂ）と２本の１２８ビットのデータ線（ａ，ｂ）とで接続されている。

【００３０】クロスバスイッチ側アドレス制御部６１－１は２つのポートからのアドレスを入力し、プロセッサボード２－１にアドレス及び識別ビットを出力する。尚、図示していないが、他のクロスバスイッチ側入出力部６－２～６－４も上記のクロスバスイッチ側入出力部６－１と同様の構成となっている。

【００３１】図３は図１のデータ部７－１の構成を示すブロック図である。図において、データ部７－１はボード内スイッチ７１－１と、バッファ７２－１，７３－１と、スイッチ（ＳＷ＃１～ＳＷ＃３）７４－１，７５－１，７６－１と、バッファＡ群７７－１と、バッファＢ群７８－１とから構成されている。尚、他のデータ部７－２～７－４も上記のデータ部７－１と同様の構成となっている。

【００３２】図４は図１のアドレスコントロール部８－１の構成を示すブロック図である。図において、アドレスコントロール部８－１はボード内アドレス制御部８１－１と、ボード内スイッチ制御部８２－１とを備えている。尚、他のアドレスコントロール部８－２～８－４も上記のアドレスコントロール部８－１と同様の構成となっている。

【００３３】図５は図３のボード内スイッチ７１－１の構成を示すブロック図である。図において、ボード内スイッチ７１－１はスイッチ（ＳＷ＃１１～ＳＷ＃２０）７１ａ－１～７１ｊ－１を備えている。

【００３４】図６はスイッチの構成例を示す図である。図６（ａ）は図３に示すスイッチ（ＳＷ＃２，ＳＷ＃３）７５－１，７６－１及び図５に示すスイッチ（ＳＷ＃１１～ＳＷ＃１６）７１ａ－１～７１ｆ－１の構成を示し、図６（ｂ）は図３に示すスイッチ（ＳＷ＃１）７４－１及び図５に示すスイッチ（ＳＷ＃１７～ＳＷ＃２０）７１ｇ－１～７１ｊ－１の構成を示している。

【００３５】図７は図２に示すクロスバスイッチ側アドレス制御部６１－１の構成を示すブロック図である。クロスバスイッチ側アドレス制御部６１－１はコントローラ６１ａ－１と、メモリ（Ａ）６１ｂ－１と、メモリ（Ｂ）６１ｃ－１とから構成されている。

【００３６】図８（ａ）は図７のメモリ（Ａ）６１ｂ－１の記憶内容を示す図であり、図８（ｂ）は図７のメモリ（Ｂ）６１ｃ－１の記憶内容を示す図である。これらの図において、メモリ（Ａ）６１ｂ－１にはボード名（プロセッサ＃１，プロセッサ＃２，メモリ＃１，メモリ＃２，Ｉ／Ｏ＃１，Ｉ／Ｏ＃２，Ｉ／Ｏ＃３，Ｉ／Ｏ＃４）とポート名（ａ，ｂ）とを対応付けて記憶している。

【００３７】また、メモリ（Ｂ）６１ｃ－１にはａポートの通信相手先ボード名とａポートの通信相手先ポート名とを、またｂポートの通信相手先ボード名とｂポートの通信相手先ポート名とを夫々対応付けて記憶している。

【００３８】図９は図４のボード内アドレス制御部８１

－１の構成を示すブロック図である。図において、ボード内アドレス制御部８１－１はコントローラ８１ａ－１と、メモリ（Ｃ）８１ｂ－１と、メモリ（Ｄ）８１ｃ－１と、カウンタ８１ｄ－１～８１ｇ－１とから構成されている。

【００３９】図１０（ａ）は図９のメモリ（Ｃ）８１ｂ－１の記憶内容を示す図であり、図１０（ｂ）は図９のメモリ（Ｄ）８１ｃ－１の記憶内容を示す図である。これらの図において、メモリ（Ｃ）８１ｂ－１には現在の識別ビットＳａの値及び現在の識別ビットＳｂの値と、１クロック前の識別ビットＳａの値及び１クロック前の識別ビットＳｂの値とが記憶されている。

【００４０】また、メモリ（Ｄ）８１ｃ－１にはバッファＡ群７７－１用のアドレス情報及びデータ送出順情報と、バッファＢ群７８－１用のアドレス情報及びデータ送出順情報とが記憶されている。

【００４１】ここで、アドレス情報ＡＡ１，ＡＡ２，ＡＡ３，ＡＡ４，……はバッファＡ群７７－１に入ったデータに関連して送られてきたアドレス線信号内容を示し、データ送出順情報ＮＡＡ１，ＮＡＡ２，ＮＡＡ３，ＮＡＡ４，……は対応するアドレス線信号内容と同時に送られてきたデータがブロック先頭から幾つ目のデータとして送られてきたかを示している。

【００４２】アドレス情報ＡＢ１，ＡＢ２，ＡＢ３，ＡＢ４，……はバッファＢ群７８－１に入ったデータに関連して送られてきたアドレス線信号内容を示し、データ送出順情報ＮＡＢ１，ＮＡＢ２，ＮＡＢ３，ＮＡＢ４，……は対応するアドレス線信号内容と同時に送られてきたデータがブロック先頭から幾つ目のデータとして送られてきたかを示している。

【００４３】図１１は図４のボード内スイッチ制御部８２－１による図３のスイッチ（ＳＷ＃１～ＳＷ＃３）７４－１～７６－１及び図５のスイッチ（ＳＷ＃１１～ＳＷ＃２０）７１ａ－１～７１ｊ－１の制御を示す図である。

【００４４】ボード内スイッチ制御部８２－１は図３及び図５に示すボード内スイッチ７１－１のポートａからポートｃに接続する場合（ａ→ｃ）及びポートｂからポートｄに接続する場合（ｂ→ｄ）に、スイッチ（ＳＷ＃１１）７１ａ－１とスイッチ（ＳＷ＃１３）７１ｃ－１とスイッチ（ＳＷ＃１６）７１ｆ－１とスイッチ（ＳＷ＃１８）７１ｈ－１とが“０”側に接続されるよう制御し、スイッチ（ＳＷ＃１２）７１ｂ－１とスイッチ（ＳＷ＃１７）７１ｇ－１とが“１”側に接続されるよう制御する。

【００４５】この時、スイッチ（ＳＷ＃１～ＳＷ＃３）７４－１～７６－１とスイッチ（ＳＷ＃１４）７１ｄ－１とスイッチ（ＳＷ＃１５）７１ｅ－１とスイッチ（ＳＷ＃１９）７１ｉ－１とスイッチ（ＳＷ＃２０）７１ｊ－１とは夫々“１”側及び“０”側のいずれに接続されていてもよい。図１１においてはこの状態を「－」で示している。

【００４６】ボード内スイッチ制御部８２－１はボード内スイッチ７１－１のポートａからポートｅに接続する場合（ａ→ｅ）及びポートｂからポートｆに接続する場合（ｂ→ｆ）に、スイッチ（ＳＷ＃２）７５－１とスイッチ（ＳＷ＃３）７６－１とスイッチ（ＳＷ＃１１）７１ａ－１とスイッチ（ＳＷ＃２０）７１ｊ－１とが“０”側に接続されるよう制御し、スイッチ（ＳＷ＃１２）７１ｂ－１とスイッチ（ＳＷ＃１３）７１ｃ－１とスイッチ（ＳＷ＃１６）７１ｆ－１とスイッチ（ＳＷ＃１９）７１ｉ－１とが“１”側に接続されるよう制御する。

【００４７】この時、スイッチ（ＳＷ＃１）７４－１とスイッチ（ＳＷ＃１４）７１ｄ－１とスイッチ（ＳＷ＃１５）７１ｅ－１とスイッチ（ＳＷ＃１７）７１ｇ－１とスイッチ（ＳＷ＃１８）７１ｈ－１とは夫々“１”側及び“０”側のいずれに接続されていてもよい。

【００４８】ボード内スイッチ制御部８２－１はボード内スイッチ７１－１のポートａからポートｃ，ｄに接続する場合（ａ→ｃ，ｄ）に、スイッチ（ＳＷ＃２）７５－１とスイッチ（ＳＷ＃３）７６－１とが“０”側に接続されるよう制御する。また、ボード内スイッチ制御部８２－１はクロスバスイッチ５のクロックに同期してスイッチ（ＳＷ＃１１）７１ａ－１が“１”側と“０”側とに、スイッチ（ＳＷ＃１３）７１ｃ－１が“１”側及び“０”側のいずれかと“０”側とに、スイッチ（ＳＷ＃１４）７１ｄ－１が“０”側と“１”側及び“０”側のいずれかとに、スイッチ（ＳＷ＃１７）７１ｇ－１が“１”側及び“０”側のいずれかと“１”側とに、スイッチ（ＳＷ＃１８）７１ｈ－１が“１”側と“１”側及び“０”側のいずれかとに夫々繰り返し交互に接続されるよう制御する。

【００４９】この時、スイッチ（ＳＷ＃１）７４－１とスイッチ（ＳＷ＃１２）７１ｂ－１とスイッチ（ＳＷ＃１５）７１ｅ－１とスイッチ（ＳＷ＃１６）７１ｆ－１とスイッチ（ＳＷ＃１９）７１ｉ－１とスイッチ（ＳＷ＃２０）７１ｊ－１とは夫々“１”側及び“０”側のいずれに接続されていてもよい。

【００５０】ボード内スイッチ制御部８２－１はボード内スイッチ７１－１のポートａからポートｅ，ｆに接続する場合（ａ→ｅ，ｆ）に、スイッチ（ＳＷ＃２）７５－１とスイッチ（ＳＷ＃３）７６－１とが“０”側に接続されるよう制御する。また、ボード内スイッチ制御部８２－１はクロスバスイッチ５のクロックに同期してスイッチ（ＳＷ＃１１）７１ａ－１が“１”側と“０”側とに、スイッチ（ＳＷ＃１３）７１ｃ－１が“１”側及び“０”側のいずれかと“１”側とに、スイッチ（ＳＷ＃１４）７１ｄ－１が“１”側と“１”側及び“０”側のいずれかとに、スイッチ（ＳＷ＃１９）７１ｉ－１が

“１”側及び“０”側のいずれかと“１”側とに、スイッチ（ＳＷ＃２０）７１ｊ－１が“１”側と“１”側及び“０”側のいずれかとに夫々繰り返し交互に接続されるよう制御する。

【００５１】この時、スイッチ（ＳＷ＃１）７４－１とスイッチ（ＳＷ＃１２）７１ｂ－１とスイッチ（ＳＷ＃１５～ＳＷ＃１８）７１ｅ－１～７１ｈ－１とは夫々“１”側及び“０”側のいずれに接続されていてもよい。

【００５２】ボード内スイッチ制御部８２－１はボード内スイッチ７１－１のポートｂからポートｃ，ｄに接続する場合（ｂ→ｃ，ｄ）に、スイッチ（ＳＷ＃２）７５－１とスイッチ（ＳＷ＃３）７６－１とが“０”側に接続されるよう制御する。また、ボード内スイッチ制御部８２－１はクロスバスイッチ５のクロックに同期してスイッチ（ＳＷ＃１２）７１ｂ－１が“１”側と“０”側とに、スイッチ（ＳＷ＃１５，ＳＷ＃１７）７１ｅ－１，７１ｇ－１が“１”側及び“０”側のいずれかと“０”側とに、スイッチ（ＳＷ＃１６，ＳＷ＃１８）７１ｆ－１，７１ｈ－１が“０”側と“１”側及び“０”側のいずれかとに夫々繰り返し交互に接続されるよう制御する。

【００５３】この時、スイッチ（ＳＷ＃１）７４－１とスイッチ（ＳＷ＃１１）７１ａ－１とスイッチ（ＳＷ＃１３）７１ｃ－１とスイッチ（ＳＷ＃１４）７１ｄ－１とスイッチ（ＳＷ＃１９）７１ｉ－１とスイッチ（ＳＷ＃２０）７１ｊ－１とは夫々“１”側及び“０”側のいずれに接続されていてもよい。

【００５４】ボード内スイッチ制御部８２－１はボード内スイッチ７１－１のポートｂからポートｅ，ｆに接続する場合（ｂ→ｅ，ｆ）に、スイッチ（ＳＷ＃２）７５－１とスイッチ（ＳＷ＃３）７６－１とが“０”側に接続されるよう制御する。また、ボード内スイッチ制御部８２－１はクロスバスイッチ５のクロックに同期してスイッチ（ＳＷ＃１２）７１ｂ－１が“１”側と“０”側とに、スイッチ（ＳＷ＃１５）７１ｅ－１が“１”側及び“０”側のいずれかと“１”側とに、スイッチ（ＳＷ＃１６）７１ｆ－１が“１”側と“１”側及び“０”側のいずれかとに、スイッチ（ＳＷ＃１９）７１ｉ－１が“１”側及び“０”側のいずれかと“０”側とに、スイッチ（ＳＷ＃２０）７１ｊ－１が“０”側と“１”側及び“０”側のいずれかとに夫々繰り返し交互に接続されるよう制御する。

【００５５】この時、スイッチ（ＳＷ＃１）７４－１とスイッチ（ＳＷ＃１１）７１ａ－１とスイッチ（ＳＷ＃１３）７１ｃ－１とスイッチ（ＳＷ＃１４）７１ｄ－１とスイッチ（ＳＷ＃１７）７１ｇ－１とスイッチ（ＳＷ＃１８）７１ｈ－１とは夫々“１”側及び“０”側のいずれに接続されていてもよい。

【００５６】ボード内スイッチ制御部８２－１はボード内スイッチ７１－１のポートｃ，ｄからポートａに接続する場合（ｃ，ｄ→ａ）に、スイッチ（ＳＷ＃２）７５－１とスイッチ（ＳＷ＃３）７６－１とが“１”側に接続されるよう制御する。また、ボード内スイッチ制御部８２－１はクロスバスイッチ５のクロックに同期してスイッチ（ＳＷ＃１１）７１ａ－１が“０”側と“１”側とに、スイッチ（ＳＷ＃１３）７１ｃ－１が“０”側と“１”側及び“０”側のいずれかとに、スイッチ（ＳＷ＃１４）７１ｄ－１が“１”側及び“０”側のいずれかと“０”側とに、スイッチ（ＳＷ＃１７）７１ｇ－１が“１”側と“１”側及び“０”側のいずれかとに、スイッチ（ＳＷ＃１８）７１ｈ－１が“１”側及び“０”側のいずれかと“１”側とに夫々繰り返し交互に接続されるよう制御する。

【００５７】この時、スイッチ（ＳＷ＃１）７４－１とスイッチ（ＳＷ＃１２）７１ｂ－１とスイッチ（ＳＷ＃１５）７１ｅ－１とスイッチ（ＳＷ＃１６）７１ｆ－１とスイッチ（ＳＷ＃１９）７１ｉ－１とスイッチ（ＳＷ＃２０）７１ｊ－１とは夫々“１”側及び“０”側のいずれに接続されていてもよい。

【００５８】ボード内スイッチ制御部８２－１はボード内スイッチ７１－１のポートｃ，ｄからポートｂに接続する場合（ｃ，ｄ→ｂ）に、スイッチ（ＳＷ＃２）７５－１とスイッチ（ＳＷ＃３）７６－１とが“１”側に接続されるよう制御する。また、ボード内スイッチ制御部８２－１はクロスバスイッチ５のクロックに同期してスイッチ（ＳＷ＃１２）７１ｂ－１が“０”側と“１”側とに、スイッチ（ＳＷ＃１５）７１ｅ－１が“０”側と“１”側及び“０”側のいずれかとに、スイッチ（ＳＷ＃１６）７１ｆ－１が“１”側及び“０”側のいずれかと“０”側とに、スイッチ（ＳＷ＃１９）７１ｉ－１が“０”側と“１”側及び“０”側のいずれかとに、スイッチ（ＳＷ＃２０）７１ｊ－１が“１”側及び“０”側のいずれかと“０”側とに夫々繰り返し交互に接続されるよう制御する。

【００５９】この時、スイッチ（ＳＷ＃１）７４－１とスイッチ（ＳＷ＃１１）７１ａ－１とスイッチ（ＳＷ＃１３）７１ｃ－１とスイッチ（ＳＷ＃１４）７１ｄ－１とスイッチ（ＳＷ＃１７）７１ｇ－１とスイッチ（ＳＷ＃１８）７１ｈ－１とは夫々“１”側及び“０”側のいずれに接続されていてもよい。

【００６０】ボード内スイッチ制御部８２－１はボード内スイッチ７１－１の出力側に接続される場合に、スイッチ（ＳＷ＃２）７５－１とスイッチ（ＳＷ＃３）７６－１とが“０”側に接続されるよう制御する。

【００６１】この時、スイッチ（ＳＷ＃１）７４－１とスイッチ（ＳＷ＃１１～ＳＷ＃２０）７１ａ－１～７１ｊ－１とは夫々“１”側及び“０”側のいずれに接続されていてもよい。

【００６２】ボード内スイッチ制御部８２－１はボード

内スイッチ７１－１の入力側に接続される場合に、スイッチ（ＳＷ＃２）７５－１とスイッチ（ＳＷ＃３）７６－１とが“１”側に接続されるよう制御する。

【００６３】この時、スイッチ（ＳＷ＃１）７４－１とスイッチ（ＳＷ＃１１～ＳＷ＃２０）７１ａ－１～７１ｊ－１とは夫々“１”側及び“０”側のいずれに接続されていてもよい。

【００６４】ボード内スイッチ制御部８２－１はボード内スイッチ７１－１がバッファＡ群７７－１の出力に接続される場合に、スイッチ（ＳＷ＃１）７４－１が“１”側に接続されるよう制御する。

【００６５】この時、スイッチ（ＳＷ＃２，ＳＷ＃３）７５－１，７６－１とスイッチ（ＳＷ＃１１～ＳＷ＃２０）７１ａ－１～７１ｊ－１とは夫々“１”側及び“０”側のいずれに接続されていてもよい。

【００６６】ボード内スイッチ制御部８２－１はボード内スイッチ７１－１がバッファＢ群７８－１の出力に接続される場合に、スイッチ（ＳＷ＃１）７４－１が“０”側に接続されるよう制御する。

【００６７】この時、スイッチ（ＳＷ＃２，ＳＷ＃３）７５－１，７６－１とスイッチ（ＳＷ＃１１～ＳＷ＃２０）７１ａ－１～７１ｊ－１とは夫々“１”側及び“０”側のいずれに接続されていてもよい。

【００６８】これら図１～図１１を参照して本発明の一実施例によるクロスバスイッチ装置１について説明する。Ｉ／Ｏボード（＃１～＃４）４－１～４－４はクロスバスイッチ５の各ポートに接続され、クロスバスイッチ５の１ポート分のみを使用している。

【００６９】これに対し、プロセッサボード２－１，２－２及びメモリボード３－１，３－２は図２に示すクロスバスイッチ側入出力部６－１～６－４を介してクロスバスイッチ５の各ポートに接続され、クロスバスイッチ５の２ポート分を使用している。

【００７０】クロスバスイッチ側入出力部６－１～６－４は図３及び図４に示す各ボード内のデータ部７－１～７－４及びアドレスコントロール部８－１～８－４に接続されている。クロスバスイッチ側入出力部６－１～６－４では従来のクロスバスイッチ経由での転送要求に対し、識別ビットによって空きポートを確認した後に転送の可否を返答したり、接続されたボードからの転送要求を受けて適切なボードが接続されたクロスバスイッチ側アドレス制御部６１－１に転送要求を行う。

【００７１】図３に示す各ボード内のデータ部７－１～７－４はデータ振り分け用スイッチ７４－１，７５－１，７６－１と２系統のバッファＡ群７７－１及びバッファＢ群７８－１とからなる。図４に示す各ボード内のアドレスコントロール部８－１～８－４はボード内アドレス制御部８１－１とボード内スイッチ制御部８２－１とからなる。

【００７２】データ部７－１～７－４のボード内スイッチ７１－１は図５に示す複数のスイッチ７１ａ－１～７１ｊ－１の相互接続からなり、ボード内スイッチ制御部８２－１からの指示に基づいて各スイッチ７１ａ－１～７１ｊ－１が切替えられる。バッファＡ群７７－１及びバッファＢ群７８－１は各ボードへの入力データをポート毎にまとめて従来のボードがデータ幅を意識すること無く、データを受け取ることができるようにデータを２５６ビット幅で保持する。

【００７３】アドレスコントロール部８－１～８－４のボード内アドレス制御部８１－１は、図９に示すように、クロスバスイッチ５へのアドレス線と、識別ビット線（Ｓａ，Ｓｂ）と、ａ，ｂポート識別線と、図４０に示す従来装置のコントローラ２２－１への信号線と、バッファＡ群７７－１及びバッファＢ群７８－１へのデータ取り込みタイミング用信号線と、その前段の１２８ビットバッファ７２－１，７３－１へのデータ取り込みタイミング用信号線と、従来装置の入力バッファ２３－１へのデータ取り込みタイミング用信号線とに夫々接続されている。

【００７４】ボード内アドレス制御部８１－１は従来装置のコントローラ２２－１からの転送要求を受けて識別ビットを更新し、クロスバスイッチ５側に転送要求を行う。また、ボード内アドレス制御部８１－１はクロスバスイッチ５側からの転送要求を受けて識別ビットの情報から転送されるデータの幅とポートとを認識してバッファＡ群７７－１及びバッファＢ群７８－１へデータを取込み、従来装置のデータ入出力部の空きのタイミングでそのデータを転送する。

【００７５】ボード内スイッチ制御部８２－１はボード内アドレス制御部８１－１からの指示を受けると、図１１に示す内容を参照し、必要なスイッチに対して切替え指示を行う。

【００７６】図７を参照すると、図２に示すクロスバスイッチ側入出力部６－１内のアドレス制御部６１－１の構成が示されており、アドレス制御部６１－１はコントローラ６１ａ－１とメモリ（Ａ）６１ｂ－１とメモリ（Ｂ）６１ｃ－１とから構成されている。

【００７７】メモリ（Ａ）６１ｂ－１はクロスバスイッチ装置１全体の構成環境を記憶しており［図８（ａ）参照］、該当する通信相手が２５６ビット幅転送の可能性があるかどうかを知るための手段となる。メモリ（Ｂ）６１ｃ－１は現在通信中の相手のボード名とポート名とを記憶し［図８（ｂ）参照］、アドレス線の信号を伝達する際に参照する。

【００７８】図９を参照すると、図４に示すボード内アドレス制御部８１－１の詳細な構成が示されており、ボード内アドレス制御部８１－１はコントローラ８１ａ－１と、メモリ（Ｃ）８１ｂ－１と、メモリ（Ｄ）８１ｃ－１と、カウンタ８１ｄ－１～８１ｇ－１とから構成されている。

【００７９】メモリ（Ｃ）８１ｂ－１は識別ビットＳａ，Ｓｂの１クロック前の値を保持し［図１０（ａ）参照］、該当クロックで値が変化したものをコントローラ８１ａ－１が知るための手段となる。

【００８０】メモリ（Ｄ）８１ｃ－１はデータ部７－１のバッファＡ群７７－１とバッファＢ群７８－１とのデータとともに送付されたアドレス信号内容ＡＡ１，ＡＡ２，ＡＡ３，ＡＡ４，……，ＡＢ１，ＡＢ２，ＡＢ３，ＡＢ４，……を、同時に送られたデータを特定する記録ＮＡＡ１，ＮＡＡ２，ＮＡＡ３，ＮＡＡ４，……，ＮＡＢ１，ＮＡＢ２，ＮＡＢ３，ＮＡＢ４，……とともに保持する［図１０（ｂ）参照］。

【００８１】カウンタ８１ｄ－１～８１ｇ－１はバッファＡ群７７－１及びバッファＢ群７８－１に夫々どれだけのデータが入っているかと、従来装置のデータ入力部にブロックの何番目のデータを提供しているかを示す。

【００８２】これはバッファＡ群７７－１及びバッファＢ群７８－１にデータ取り込み用クロックを送る時に、同時に該当するカウンタ８１ｄ－１，８１ｆ－１にカウントアップ指示を出力し、従来装置のデータ入力部のバッファにデータ取り込み指示を送る時に、同時にカウンタ８１ｄ－１，８１ｆ－１にカウントダウン指示を、カウンタ８１ｅ－１，８１ｇ－１にカウントアップ指示を夫々出力し、従来装置のデータ入力部のバッファへのブロックデータの最後のデータ取り込み指示とともにカウンタ８１ｅ－１，８１ｇ－１にゼロリセット指示を送ることで実現される。

【００８３】図１２～図１５は図２及び図７に示すクロスバスイッチ側アドレス制御部６１－１の動作を示すフローチャートであり、図１６～図２３は図４及び図９に示すボード内アドレス制御部８１－１の動作を示すフローチャートである。

【００８４】これら図１～図２３を参照して本発明の一実施例によるクロスバスイッチ装置１の動作について説明する。尚、上記のフローチャートの動作は各制御部が図示せぬ制御メモリのプログラムを実行することでも実現可能であり、制御メモリとしてはＲＯＭ（リードオンリメモリ）等が使用可能である。

【００８５】図１２～図１５はクロスバスイッチ側アドレス制御部６１－１に直接接続されたプロセッサボード２－１が転送要求を行う場合の動作を示している。この場合、クロスバスイッチ側アドレス制御部６１－１はプロセッサボード２－１のアドレスコントロール部８－１のボード内アドレス制御部８１－１からアドレス線を介して転送要求を受領すると（図１２ステップＳ１）、接続されているプロセッサボード２－１が２５６ビットボードであれば（図１２ステップＳ２）、識別ビットを参照し、自回路のポートの空き状況を確認する（図１２ステップＳ３）。

【００８６】クロスバスイッチ５のポートを２５６ビット確保できれば、つまりクロスバスイッチ側入出力部６－１が接続されるクロスバスイッチ５の２つのポートを確保できれば（図１２ステップＳ４）、クロスバスイッチ側アドレス制御部６１－１はメモリ（Ａ）６１ｂ－１を参照し、通信相手の最大データ幅を確認する（図１２ステップＳ５）。

【００８７】クロスバスイッチ側アドレス制御部６１－１はその通信相手の最大データ幅が２５６ビット幅であれば（図１２ステップＳ６）、通信相手のポートａ，ｂに対応する２本のアドレス線に転送要求を送付し（図１２ステップＳ７）、１２８ビットであれば通信相手のポートに対応するアドレス線（１本）に転送要求を送付する（図１２ステップＳ１２）。

【００８８】クロスバスイッチ側アドレス制御部６１－１は２本のアドレス線の両方から転送ＯＫが返ってくると（図１２ステップＳ８）、その信号をプロセッサボード２－１のボード内アドレス制御部８１－１に中継する。クロスバスイッチ側アドレス制御部６１－１は以降、転送終了まで同じ経路で信号を中継する（図１２ステップＳ９）。

【００８９】これに対し、クロスバスイッチ側アドレス制御部６１－１は１本のアドレス線のみから転送ＯＫがあった場合（図１４ステップＳ１８）、予め決められた方法でいずれかのポートに対応する識別ビットを“０”に変更する（図１４ステップＳ１９）。

【００９０】クロスバスイッチ側アドレス制御部６１－１は識別ビットが“１”の側の経路を確保して転送ＯＫ信号をプロセッサボード２－１のボード内アドレス制御部８１－１に中継する（図１４ステップＳ２０）。

【００９１】この場合、クロスバスイッチ側アドレス制御部６１－１はメモリ（Ｂ）６１ｃ－１に確保した経路と相手先情報とを記録し（図１４ステップＳ２０）、以降、ボード内アドレス制御部８１－１からの信号についてメモリ（Ｂ）６１ｃ－１に記録した経路と相手先情報とを参照して確認し、同じ通信相手からの信号であれば、転送終了までその信号の中継を続ける（図１４ステップＳ２１）。尚、クロスバスイッチ側アドレス制御部６１－１は転送終了になると、同時にメモリ（Ｂ）６１ｃ－１の経路情報を消去する（図１４ステップＳ２２）。

【００９２】クロスバスイッチ側アドレス制御部６１－１は両方のアドレス線から転送不可が返ってきた場合（図１４ステップＳ２３）、その信号をプロセッサボード２－１のボード内アドレス制御部８１－１に中継する（図１４ステップＳ２４）。

【００９３】一方、クロスバスイッチ側アドレス制御部６１－１はプロセッサボード２－１のポートが１２８ビット幅しか確保できなければ（図１２ステップＳ１０）、相手のアドレス線１本を予め決められた方法で選択して転送要求を送付する（図１２ステップＳ１１）。

【００９４】クロスバスイッチ側アドレス制御部６１－１はその転送要求に対して転送ＯＫが返ってくると（図１４ステップＳ１８）、上記と同様にして経路を確保し（図１４ステップＳ２０）、プロセッサボード２－１のボード内アドレス制御部８１－１に転送ＯＫを中継する（図１４ステップＳ２１）。

【００９５】この場合も、クロスバスイッチ側アドレス制御部６１－１はメモリ（Ｂ）６１ｃ－１に確保した経路と相手先情報とを記録し（図１４ステップＳ２０）、以降、ボード内アドレス制御部８１－１からの信号についてメモリ（Ｂ）６１ｃ－１に記録した経路と相手先情報とを参照して確認し、同じ通信相手からの信号であれば、転送終了までその信号の中継を続ける（図１４ステップＳ２１）。尚、クロスバスイッチ側アドレス制御部６１－１は転送終了になると、同時にメモリ（Ｂ）６１ｃ－１の経路情報を消去する（図１４ステップＳ２２）。

【００９６】クロスバスイッチ側アドレス制御部６１－１は転送不可が返ってきた場合にも（図１４ステップＳ２３）、その信号を同じボード内アドレス制御部８１－１に中継する（図１４ステップＳ２４）。

【００９７】プロセッサボード２－１のポートが２５６ビットでない場合（図１２ステップＳ２）、クロスバスイッチ側アドレス制御部６１－１はメモリ（Ａ）６１ｂ－１を参照し、通信相手のデータ幅に応じたアドレス線に転送要求の信号を中継する（図１３ステップＳ１３）。

【００９８】クロスバスイッチ側アドレス制御部６１－１はその転送要求に対して転送ＯＫが返ってくると（図１３ステップＳ１４）、上記と同様に、プロセッサボード２－１のボード内アドレス制御部８１－１に転送ＯＫを中継する。以降、クロスバスイッチ側アドレス制御部６１－１は転送終了までその信号の中継を続ける（図１３ステップＳ１５）。

【００９９】クロスバスイッチ側アドレス制御部６１－１は転送不可が返ってきた場合にも（図１３ステップＳ１６）、その信号を同じボード内アドレス制御部８１－１に中継する（図１３ステップＳ１７）。

【０１００】図１５はクロスバスイッチ側アドレス制御部６１－１がクロスバスイッチ５側から転送要求を受けた場合の動作を示している。この場合、クロスバスイッチ側アドレス制御部６１－１はクロスバスイッチ５側から転送要求を受領すると（図１５ステップＳ３１）、識別ビットを参照し、自回路のポートの空き状況を確認する（図１５ステップＳ３２）。

【０１０１】クロスバスイッチ側アドレス制御部６１－１は接続されているプロセッサボード２－１が２５６ビットボードであれば（図１５ステップＳ３３）、転送要求がアドレス線２本からきたかどうかを判定する（図１５ステップＳ３４）。

【０１０２】クロスバスイッチ側アドレス制御部６１－１は転送要求がアドレス線２本からきていれば、転送要求のポートが確保できるかどうかを調査する（図１５ステップＳ３５）。クロスバスイッチ側アドレス制御部６１－１は転送要求のポートを確保可能であれば、識別ビットＳａ，Ｓｂを両方“１”に変更することで確保し（図１５ステップＳ３６）、確保できた識別ビットに対応するアドレス線を介して転送ＯＫを返す（図１５ステップＳ３７）。

【０１０３】クロスバスイッチ側アドレス制御部６１－１は転送要求をボード内アドレス制御部８１－１に転送し（図１５ステップＳ３８）、メモリ（Ｂ）６１ｃ－１に転送経路と相手情報とを記憶し、以降該当アドレス線からの信号はメモリ（Ｂ）６１ｃ－１の内容を参照し、該当ポートからの信号であればこれをボード内アドレス制御部８１－１に中継する（図１５ステップＳ３９）。

【０１０４】このとき、ボード内アドレス制御部８１－１は１ビットのａ，ｂポート識別線が“０”の時にａポートのデータ転送先からのアドレス信号であり、“１”の時にｂポートのデータ転送先からのアドレス信号であると識別する。

【０１０５】転送終了後、クロスバスイッチ側アドレス制御部６１－１はメモリ（Ｂ）６１ｃ－１の内容をクリアし、“１”に変更した識別ビットを元に戻す（図１５ステップＳ４０）。

【０１０６】クロスバスイッチ側アドレス制御部６１－１は接続されているプロセッサボード２－１が１２８ビットボードで（図１５ステップＳ３３）、対応するポートが空いていれば（図１５ステップＳ４１）、転送要求をそのまま中継し、従来装置の空き状況に対する返答を中継して返す（図１５ステップＳ４２）。以降、クロスバスイッチ側アドレス制御部６１－１は上記と同様の動作を行う（図１５ステップＳ３８～Ｓ４０）。

【０１０７】クロスバスイッチ側アドレス制御部６１－１は対応するポートが空いていなければ（図１５ステップＳ４１）、あるいは転送要求がアドレス線２本からきていない時にポートが空いていなければ（図１５ステップＳ３４，Ｓ４３）、または転送要求のポートが確保できなければ（図１５ステップＳ４４）、転送要求のあった経路で転送不可を返す（図１５ステップＳ４７）。

【０１０８】クロスバスイッチ側アドレス制御部６１－１は転送要求がアドレス線２本からこない時に、転送要求のポートが確保できれば（図１５ステップＳ４３）、あるいは転送要求がアドレス線２本からきている時に、転送要求のポートが１本確保できれば（図１５ステップＳ４４）、空きポートに対応する識別ビットを“１”に変更する（図１５ステップＳ４５）。

【０１０９】クロスバスイッチ側アドレス制御部６１－１は確保できたポートに対応するアドレス線を使用して転送ＯＫを返し（図１５ステップＳ４６）、以降、上記

と同様の動作を行う（図15ステップS38～S40）。

【0110】図16～図23にプロセッサボード2－のアドレスコントローラ部8－1のボード内アドレス制御部81－1（128ビットボードには実装されていない）の動作を示す。この場合、ボード内アドレス制御部81－1は直接接続された従来装置のコントローラ22－1（図40参照）から転送要求を受けると（図16ステップS51）、プロセッサボード2－1のデータ部7－1のボード内スイッチ71－1のポートc，dが使用されていないことを確認し、そのまま転送要求を中継する（図16ステップS52）。もし使用されていた場合は転送不可をコントローラ22－1に返す。

【0111】その後、ボード内アドレス制御部81－1は転送先からの転送OK通知を受領して識別ビットを確認し（図17ステップS61，S62）、256ビットの帯域を確保できれば、すなわちSa＝1，Sb＝1であれば（図17ステップS63）、これにデータを直接送り出せるようボード内スイッチ制御部82－1に経路を、つまりc→a，d→b経路の確保とスイッチ（SW#2，#3）75－1，76－1の送出側経路への変更とを指示する（図17ステップS64）。

【0112】その後、ボード内アドレス制御部81－1は従来装置の出力バッファ24－1（図40参照）にクロスバスイッチ5のクロックを伝達し、毎クロック、新しいデータをクロスバスイッチ5上に送出可能とする（図17ステップS65）。

【0113】ボード内アドレス制御部81－1はコントローラ22－1からのアドレス線信号を転送完了までそのまま中継し（図17ステップS66）、コントローラ22－1から転送完了信号が送られてきたのをきっかけに識別ビットSa，Sbを“0”に戻す（図17ステップS67）。

【0114】ボード内アドレス制御部81－1は128ビットだけ帯域を確保できれば、すなわち識別ビットがSa＝1，Sb＝0であれば（図17ステップS68）、または識別ビットがSa＝0，Sb＝1であれば（図18ステップS74）、c，dから順番にデータを送れるようボード内スイッチ制御部82－1にクロック毎に経路を切替えるモードで動作するよう指示する。

【0115】識別ビットがSa＝1，Sb＝0の場合、ボード内アドレス制御部81－1はボード内スイッチ制御部82－1にc→a経路の確保とスイッチ（SW#2，#3）75－1，76－1の送出側への変更とを指示する（図17ステップS69）。

【0116】以降、ボード内アドレス制御部81－1はクロスバスイッチ5のクロック毎に、c→aの経路とd→aの経路とを切替えるようにボード内スイッチ制御部82－1に指示する（図17ステップS70）。ボード内アドレス制御部81－1は従来装置の出力バッファ24－1にクロスバスイッチ5のクロックを2回に1回伝達し、2クロックに1回新しいデータをクロスバスイッチ5上に送出可能とする（図17ステップS71）。

【0117】ボード内アドレス制御部81－1はコントローラ22－1からのアドレス線信号を転送完了までそのまま中継し（図17ステップS72）、コントローラ22－1から転送完了信号が送られてきたのをきっかけに識別ビットSaを“0”に戻す（図17ステップS73）。

【0118】識別ビットがSa＝0，Sb＝1の場合、ボード内アドレス制御部81－1はボード内スイッチ制御部82－1にc→b経路の確保とスイッチ（SW#2，#3）75－1，76－1の送出側への変更とを指示する（図18ステップS75）。

【0119】以降、ボード内アドレス制御部81－1はクロスバスイッチ5のクロック毎に、c→bの経路とd→bの経路とを切替えるようにボード内スイッチ制御部82－1に指示する（図18ステップS76）。ボード内アドレス制御部81－1は従来装置の出力バッファ24－1にクロスバスイッチ5のクロックを2回に1回伝達し、2クロックに1回新しいデータをクロスバスイッチ5上に送出可能とする（図18ステップS77）。

【0120】ボード内スイッチ制御部82－1はコントローラ22－1からのアドレス線信号を転送完了までそのまま中継し（図18ステップS78）、コントローラ22－1から転送完了信号が送られてきたのをきっかけに識別ビットSbを“0”に戻す（図18ステップS79）。

【0121】ボード内アドレス制御部81－1は上記の帯域を確保できなければ、従来装置のコントローラ22－1に転送不可を中継し、再送等は従来装置にまかせる（図18ステップS80）。

【0122】図19～図23はボード内アドレス制御部81－1がクロスバスイッチ5を経由して従来装置のコントローラ22－1から転送要求を受けた場合の動作を示している。この場合、ボード内アドレス制御部81－1はメモリ（C）81b－1を参照し、1クロック前と比べて“1”に変化した識別ビットを調査し（図19ステップS91，S92）、データが送られてくるポートを認識する。

【0123】ボード内アドレス制御部81－1はこの情報と使用中の経路の確認とから判明する使用可能なバッファA群77－1またはバッファB群78－1を選択し、適切な経路をボード内スイッチ制御部82－1に指示する。

【0124】この時、128ビットずつデータが送られてくる場合は前段のバッファ72－1，73－1とバッファA群77－1またはバッファB群78－1とにクロックを交互に送ることで、256ビットのデータに揃えてバッファA群77－1またはバッファB群78－1に

記憶していく。

【０１２５】これと並行して、一方ではボード内アドレス制御部８１－１が直接接続されているコントローラ２２－１にデータを受領させるために転送要求を送出する。もし、コントローラ２２－１がもう一方のバッファ群からデータを転送中等のためデータを受領できない場合は転送要求を繰り返す。

【０１２６】転送ＯＫが返ってきたら、ボード内アドレス制御部８１－１は該当バッファ側へスイッチ（ＳＷ＃１）７４－１を切替えさせ、同時に従来装置の入力バッファ２３－１（図４０参照）へのクロック送付を開始し、バッファ内のデータを取り込ませる。但し、このクロックはカウンタ８１ｄ－１～８１ｇ－１を参照しながら該当バッファに２５６ビットのデータが存在する時のみ送付する。

【０１２７】データ部７－１のバッファにデータを格納する時のボード内アドレス制御部８１－１からバッファに制御信号を送る動作について以下に示す。転送相手と２５６ビット幅でデータを転送している場合、ボード内アドレス制御部８１－１は該当バッファ群と前段の１２８ビットバッファにデータ取り込み信号を、クロスバスイッチ５側のクロックと同期して送付する。同時に、ボード内アドレス制御部８１－１のカウンタ８１ｄ－１またはカウンタ８１ｅ－１のいずれか該当する方をカウントアップする。

【０１２８】同様に、１２８ビットでデータを受けている場合、ボード内アドレス制御部８１－１は最初に受領する下位１２８ビットのタイミングで該当する前段バッファに取り込み指示を送り、クロスバスイッチ５側の次のクロックタイミングで該当バッファ群に信号を送付して古いデータを押し下げるとともに、ボード内スイッチ７１－１を介して直接見える上位１２８ビットと前段バッファが持つ下位１２８ビット分のデータとをあわせて新たなデータとして取り込む。同時に、ボード内アドレス制御部８１－１のカウンタ８１ｄ－１またはカウンタ８１ｅ－１の該当する方をカウントアップする。

【０１２９】データ部７－１のバッファから直接接続された従来装置のデータ入力部へのデータ転送は、該当データブロックへのコントローラ２２－１からの転送ＯＫの信号を直接接続されたボード内アドレス制御部８１－１が受領した後に行う。

【０１３０】このデータ転送はカウンタ８１ｄ－１～８１ｇ－１を参照し、バッファ群に２５６ビットのデータが蓄積されている場合は予め定められた通常のクロック信号を従来装置のデータ入力部のバッファのクロック線に送る。そのバッファ群に２５６ビットのデータが無い場合はクロック信号の伝達を見送る。

【０１３１】すなわち、ボード内アドレス制御部８１－１は転送相手と２５６ビット幅でデータを転送している場合、つまり識別ビットがＳａ＝０→１，Ｓｂ＝０→１と変化している場合（図１９ステップＳ９３）、ボード内スイッチ制御部８２－１にａ→ｃ，ｂ→ｄ経路の確保とスイッチ（ＳＷ＃２，＃３）７５－１，７６－１の送出側経路への変更とを指示する（図１９ステップＳ９４）。

【０１３２】ボード内アドレス制御部８１－１は従来装置のコントローラ２２－１への転送要求がＯＫであれば（図１９ステップＳ９５）、ボード内スイッチ制御部８２－１にスイッチ（ＳＷ＃１）７４－１をバッファＡ群７７－１に切替えるよう指示する（図１９ステップＳ９６）。ボード内アドレス制御部８１－１は従来装置のコントローラ２２－１への転送要求がＮＧであれば（図１９ステップＳ９５）、アドレス線の転送要求をメモリ（Ｄ）８１ｃ－１のバッファＡ群７７－１用のアドレス用バッファに蓄積する（図１９ステップＳ９９）。

【０１３３】ボード内アドレス制御部８１－１はメモリ（Ｄ）８１ｃ－１の記録ＮＡＡｎ（ｎ＝１，２，３，４，……）とクロック信号とを参照し、アドレス情報ＡＡｎを対応するデータと同時に従来装置のコントローラ２２－１に中継し、クロスバスイッチ５の動作クロックをそのまま毎回、従来装置の入力バッファ２３－１に伝達する（図１９ステップＳ９７）。ボード内アドレス制御部８１－１はコントローラ２２－１から転送完了信号が送られてきたのをきっかけに識別ビットＳａ，Ｓｂを“０”に戻す（図１９ステップＳ９８）。

【０１３４】また、ボード内アドレス制御部８１－１は転送相手と１２８ビット幅でデータを転送している場合、つまり識別ビットがＳａ＝０→１と変化している場合（図２０ステップＳ１００）、ポートｂの接続経路を確認する（図２０ステップＳ１０１）。

【０１３５】ボード内アドレス制御部８１－１はポートｂがバッファＡ群７７－１に接続されていれば（図２０ステップＳ１０２）、ボード内スイッチ制御部８２－１にａ→ｅ，ｆ経路の確保に変更するよう指示する（図２０ステップＳ１０３）。

【０１３６】ボード内アドレス制御部８１－１は従来装置のコントローラ２２－１への転送要求がＯＫであれば（図２０ステップＳ１０４）、ボード内スイッチ制御部８２－１にスイッチ（ＳＷ＃１）７４－１をバッファＢ群７８－１に切替えるよう指示する（図２０ステップＳ１０５）。ボード内アドレス制御部８１－１は従来装置のコントローラ２２－１への転送要求がＮＧであれば（図２０ステップＳ１０４）、アドレス線の転送要求をメモリ（Ｄ）８１ｃ－１のバッファＢ群７８－１用のアドレス用バッファに蓄積する（図２０ステップＳ１０９）。

【０１３７】ボード内アドレス制御部８１－１はバッファＢ群７８－１に２５６ビット幅のデータがあれば（図２０ステップＳ１０６）、メモリ（Ｄ）８１ｃ－１の記録ＮＡＢｎ（ｎ＝１，２，３，４，……）とクロック信

号とを参照し、アドレス情報ＡＢｎを対応するデータと同時に従来装置のコントローラ２２－１に中継し、クロスバスイッチ５の動作クロックをそのまま毎回、従来装置の入力バッファ２３－１に伝達する（図２０ステップＳ１０７）。ボード内アドレス制御部８１－１はコントローラ２２－１から転送完了信号が送られてきたのをきっかけに識別ビットＳａを“０”に戻す（図２０ステップＳ１０８）。

【０１３８】ボード内アドレス制御部８１－１はポートｂがバッファＡ群７７－１に接続されていなければ（図２０ステップＳ１０２）、ボード内スイッチ制御部８２－１にａ→ｃ，ｄ経路の確保とスイッチ（ＳＷ＃２，＃３）７５－１，７６－１の送出側経路への変更とを指示する（図２２ステップＳ１１９）。

【０１３９】ボード内アドレス制御部８１－１は従来装置のコントローラ２２－１への転送要求がＯＫであれば（図２２ステップＳ１２０）、ボード内スイッチ制御部８２－１にスイッチ（ＳＷ＃１）７４－１をバッファＡ群７７－１に切替えるよう指示する（図２２ステップＳ１２１）。ボード内アドレス制御部８１－１は従来装置のコントローラ２２－１への転送要求がＮＧであれば（図２２ステップＳ１２０）、アドレス線の転送要求をメモリ（Ｄ）８１ｃ－１のバッファＡ群７７－１用のアドレス用バッファに蓄積する（図２２ステップＳ１２５）。

【０１４０】ボード内アドレス制御部８１－１はバッファＡ群７７－１に２５６ビット幅のデータがあれば（図２２ステップＳ１２２）、メモリ（Ｄ）８１ｃ－１の記録ＮＡＡｎ（ｎ＝１，２，３，４，……）とクロック信号とを参照し、アドレス情報ＡＡｎを対応するデータと同時に従来装置のコントローラ２２－１に中継し、クロスバスイッチ５の動作クロックをそのまま毎回、従来装置の入力バッファ２３－１に伝達する（図２２ステップＳ１２３）。ボード内アドレス制御部８１－１はコントローラ２２－１から転送完了信号が送られてきたのをきっかけに識別ビットＳａを“０”に戻す（図２２ステップＳ１２４）。

【０１４１】ボード内アドレス制御部８１－１は転送相手と１２８ビット幅でデータを転送している場合、つまり識別ビットがＳｂ＝０→１と変化している場合（図２１ステップＳ１１０）、ポートａがバッファＡ群７７－１に接続されていれば（図２１ステップＳ１１１）、ボード内スイッチ制御部８２－１にａ→ｅ，ｆ経路の確保に変更するよう指示する（図２１ステップＳ１１２）。

【０１４２】ボード内アドレス制御部８１－１は従来装置のコントローラ２２－１への転送要求がＯＫであれば（図２１ステップＳ１１３）、ボード内スイッチ制御部８２－１にスイッチ（ＳＷ＃１）７４－１をバッファＢ群７８－１に切替えるよう指示する（図２１ステップＳ１１４）。ボード内アドレス制御部８１－１は従来装置のコントローラ２２－１への転送要求がＮＧであれば（図２１ステップＳ１１３）、アドレス線の転送要求をメモリ（Ｄ）８１ｃ－１のバッファＢ群７８－１用のアドレス用バッファに蓄積する（図２１ステップＳ１１８）。

【０１４３】ボード内アドレス制御部８１－１はバッファＢ群７８－１に２５６ビット幅のデータがあれば（図２１ステップＳ１１５）、メモリ（Ｄ）８１ｃ－１の記録ＮＡＢｎ（ｎ＝１，２，３，４，……）とクロック信号とを参照し、アドレス情報ＡＢｎを対応するデータと同時に従来装置のコントローラ２２－１に中継し、クロスバスイッチ５の動作クロックをそのまま毎回、従来装置の入力バッファ２３－１に伝達する（図２１ステップＳ１１６）。ボード内アドレス制御部８１－１はコントローラ２２－１から転送完了信号が送られてきたのをきっかけに識別ビットＳｂを“０”に戻す（図２１ステップＳ１１７）。

【０１４４】ボード内アドレス制御部８１－１はポートａがバッファＡ群７７－１に接続されていなければ（図２１ステップＳ１１１）、ボード内スイッチ制御部８２－１にａ→ｃ，ｄ経路の確保とスイッチ（ＳＷ＃２，＃３）７５－１，７６－１の送出側経路への変更とを指示する（図２３ステップＳ１２６）。

【０１４５】ボード内アドレス制御部８１－１は従来装置のコントローラ２２－１への転送要求がＯＫであれば（図２３ステップＳ１２７）、ボード内スイッチ制御部８２－１にスイッチ（ＳＷ＃１）７４－１をバッファＡ群７７－１に切替えるよう指示する（図２３ステップＳ１２８）。ボード内アドレス制御部８１－１は従来装置のコントローラ２２－１への転送要求がＮＧであれば（図２３ステップＳ１２７）、アドレス線の転送要求をメモリ（Ｄ）８１ｃ－１のバッファＡ群７７－１用のアドレス用バッファに蓄積する（図２３ステップＳ１３２）。

【０１４６】ボード内アドレス制御部８１－１はバッファＡ群７７－１に２５６ビット幅のデータがあれば（図２３ステップＳ１２９）、メモリ（Ｄ）８１ｃ－１の記録ＮＡＡｎ（ｎ＝１，２，３，４，……）とクロック信号とを参照し、アドレス情報ＡＡｎを対応するデータと同時に従来装置のコントローラ２２－１に中継し、クロスバスイッチ５の動作クロックをそのまま毎回、従来装置の入力バッファ２３－１に伝達する（図２３ステップＳ１３０）。ボード内アドレス制御部８１－１はコントローラ２２－１から転送完了信号が送られてきたのをきっかけに識別ビットＳｂを“０”に戻す（図２３ステップＳ１３１）。

【０１４７】図２４は本発明の一実施例によるクロスバスイッチ装置１におけるデータ転送の場合分けを示す図である。図において、Ｃ１は２５６ビットのデータを２５６ビットポートへ転送する際に、２５６ビット帯域を

確保できる場合を示し、Ｃ２は２５６ビットのデータを２５６ビットポートへ転送する際に、１２８ビット帯域を確保できる場合を示し、Ｃ３は２５６ビットのデータを２５６ビットポートへ転送する際に、帯域を確保できない場合を示している。

【０１４８】Ｃ４は１２８ビットのデータを２５６ビットポートへ転送する際に、１２８ビット帯域を確保できる場合を示し、Ｃ５は１２８ビットのデータを２５６ビットポートへ転送する際に、帯域を確保できない場合を示している。

【０１４９】Ｃ６は２５６ビットのデータを１２８ビットポートへ転送する際に、１２８ビット帯域を確保できる場合を示し、Ｃ７は２５６ビットのデータを１２８ビットポートへ転送する際に、帯域を確保できない場合を示している。

【０１５０】Ｃ８は１２８ビットのデータを１２８ビットポートへ転送する際に、１２８ビット帯域を確保できる場合を示し、Ｃ９は１２８ビットのデータを１２８ビットポートへ転送する際に、帯域を確保できない場合を示している。

【０１５１】図２５は本発明の一実施例による２５６ビットのデータを２５６ビットポートへ転送する際に２５６ビット帯域を確保できる場合（Ｃ１の場合）の要求側の動作を示す図であり、図２６は本発明の一実施例による２５６ビットのデータを２５６ビットポートへ転送する際に２５６ビット帯域を確保できる場合（Ｃ１の場合）の供給側の動作を示す図である。

【０１５２】図２７は本発明の一実施例による２５６ビットのデータを２５６ビットポートへ転送する際に１２８ビット帯域を確保できる場合（Ｃ２の場合）の要求側の動作を示す図であり、図２８は本発明の一実施例による２５６ビットのデータを２５６ビットポートへ転送する際に１２８ビット帯域を確保できる場合（Ｃ２の場合）の供給側の動作を示す図である。

【０１５３】図２９は本発明の一実施例による２５６ビットのデータを２５６ビットポートへ転送する際に帯域を確保できない場合（Ｃ３の場合）の要求側の動作を示す図であり、図３０は本発明の一実施例による２５６ビットのデータを２５６ビットポートへ転送する際に帯域を確保できない場合（Ｃ３の場合）の供給側の動作を示す図である。

【０１５４】図３１は本発明の一実施例による１２８ビットのデータを２５６ビットポートへ転送する際に１２８ビット帯域を確保できる場合（Ｃ４の場合）の要求側の動作を示す図であり、図３２は本発明の一実施例による１２８ビットのデータを２５６ビットポートへ転送する際に１２８ビット帯域を確保できる場合（Ｃ４の場合）の供給側の動作を示す図である。

【０１５５】図３３は本発明の一実施例による１２８ビットのデータを２５６ビットポートへ転送する際に帯域を確保できない場合（Ｃ５の場合）の要求側の動作を示す図であり、図３４は本発明の一実施例による１２８ビットのデータを２５６ビットポートへ転送する際に帯域を確保できない場合（Ｃ５の場合）の供給側の動作を示す図である。

【０１５６】図３５は本発明の一実施例による２５６ビットのデータを１２８ビットポートへ転送する際に１２８ビット帯域を確保できる場合（Ｃ６の場合）の要求側の動作を示す図であり、図３６は本発明の一実施例による２５６ビットのデータを１２８ビットポートへ転送する際に１２８ビット帯域を確保できる場合（Ｃ６の場合）の供給側の動作を示す図である。

【０１５７】図３７は本発明の一実施例による２５６ビットのデータを１２８ビットポートへ転送する際に帯域を確保できない場合（Ｃ７の場合）の要求側の動作を示す図であり、図３８は本発明の一実施例による２５６ビットのデータを１２８ビットポートへ転送する際に帯域を確保できない場合（Ｃ７の場合）の供給側の動作を示す図である。

【０１５８】これら図１～図１１及び図２４～図３８を参照して本発明の一実施例によるクロスバスイッチ装置１を用いたデータ転送について説明する。尚、図２４に示すＣ８，Ｃ９の場合は従来装置と同じ環境であり、その動作は自明であるため、特に説明しない。

【０１５９】まず、２５６ビットのデータを２５６ビットポートへ転送する際に２５６ビット帯域を確保できる場合（Ｃ１の場合）、要求側では識別ビットＳａ，Ｓｂがともに“０”の時に従来装置のコントローラ２２－１から転送要求があると（処理Ｃ１－１）、ボード内アドレス制御部８１－１が識別ビットＳａ，Ｓｂを両方“１”にして転送要求を送出する（Ｓａ＝０→１，Ｓｂ＝０→１）（処理Ｃ１－２）。ここで、供給側では処理Ｃ－１，Ｃ－２の時に識別ビットＳａ，Ｓｂがともに“０”である。

【０１６０】その後、要求側のクロスバスイッチ側アドレス制御部６１－１は識別ビットＳａ，Ｓｂが両方“１”になると、通信相手の２つのアドレス線に転送要求を送出する。供給側のクロスバスイッチ側アドレス制御部６１－１は２つのアドレス線の転送要求を検出する。この時、識別ビットＳａ，Ｓｂは要求側で“１”、供給側で“０”である（処理Ｃ１－３）。

【０１６１】供給側のクロスバスイッチ側アドレス制御部６１－１は識別ビットＳａ，Ｓｂがともに“０”であるので、２つのアドレス線の両方に転送ＯＫを返答し、同時に識別ビットＳａ，Ｓｂを両方“１”（Ｓａ＝０→１，Ｓｂ＝０→１）にして転送要求をボードに送出する。その後、供給側のボード内アドレス制御部８１－１はボード内スイッチ制御部８２－１にａ→ｃ，ｂ→ｄの経路設定を指示する（処理Ｃ１－４）。

【０１６２】供給側のボード内アドレス制御部８１－１

は従来装置のコントローラ２２－１に転送要求を伝達する。要求側のクロスバスイッチ側アドレス制御部６１－１は２つのアドレス線の両方から転送ＯＫを確認すると、識別ビットＳａ，Ｓｂを両方“１”のままとし、ボードに転送ＯＫを伝達する（処理Ｃ１－５）。

【０１６３】要求側のボード内スイッチ制御部８２－１はボード内スイッチ制御部８２－１にａ→ｃ，ｂ→ｄの経路設定を指示し、スイッチ（ＳＷ＃２，ＳＷ＃３）７５－１，７６－１を送出側にするよう指示する（処理Ｃ１－６）。

【０１６４】要求側のボード内スイッチ制御部８２－１は指示された設定を行うと、データを送出する。供給側のボード内スイッチ制御部８２－１は送られてきたデータをバッファＡ群７７－１で受取る（処理Ｃ１－７）。

【０１６５】供給側のボード内アドレス制御部８１－１はバッファ群から従来装置のデータ入力部が取り込み中のデータがないか、または取り込み終了を確認する（処理Ｃ１－８）。

【０１６６】供給側のボード内アドレス制御部８１－１は確認後に、アドレスを従来装置のコントローラに送付する。クロスバスイッチ側アドレス制御部６１－１はスイッチ（ＳＷ＃１）７４－１をバッファＡ群７７－１に設定するよう指示する（処理Ｃ１－９）。

【０１６７】要求側のボード内アドレス制御部８１－１は送出完了後、識別ビットＳａ，Ｓｂを“０”に戻し（Ｓａ＝１→０，Ｓｂ＝１→０）、供給側のボード内アドレス制御部８１－１は転送完了後、識別ビットＳａ，Ｓｂを“０”に戻す（Ｓａ＝１→０，Ｓｂ＝１→０）（処理Ｃ１－１０）（図２５及び図２６参照）。

【０１６８】２５６ビットのデータを２５６ビットポートへ転送する際に１２８ビット帯域を確保できる場合（Ｃ２の場合）、要求側及び供給側ともに上記の処理Ｃ１－１～Ｃ１－３を行う。

【０１６９】その後に、供給側のクロスバスイッチ側アドレス制御部６１－１は識別ビットＳａ，Ｓｂをみてポートａまたはポートｂが使用中であることを認識し、空いている側のアドレス線に転送ＯＫを返答し、同時に対応する識別ビットＳａ，Ｓｂを“１”（Ｓａ＝０→１またはＳｂ＝０→１）にして転送要求をボードに送出する（処理Ｃ２－１）。

【０１７０】供給側のボード内アドレス制御部８１－１はボード内スイッチ制御部８２－１に確保したポートから確保可能なバッファ群への経路を確保するよう指示する。要求側のクロスバスイッチ側アドレス制御部６１－１は２つのアドレス線の一方から転送ＯＫを確認すると、転送ＯＫがこなかった方の識別ビットＳａ，Ｓｂを“０”にし（１，１→０または１→０，１）、ボードに転送ＯＫを伝達する（処理Ｃ２－２）。

【０１７１】要求側のボード内アドレス制御部８１－１は従来装置のコントローラ２２－１に転送ＯＫを伝達し、ボード内スイッチ制御部８２－１にスイッチ（ＳＷ＃２，ＳＷ＃３）７５－１，７６－１を送出側にするよう指示する（処理Ｃ２－３）。

【０１７２】要求側のボード内スイッチ制御部８２－１はボード内スイッチ制御部８２－１にｃ→ａ　ｏｒ　ｂ，ｄ→ａ　ｏｒ　ｂの経路設定を指示し、従来装置の出力部に新データを２クロックに１回要求する。供給側のボード内アドレス制御部８１－１は従来装置のコントローラ２２－１に転送要求を伝達し、ボード内スイッチ制御部８２－１はクロック毎にスイッチ（ＳＷ＃１１）７１ａ－１またはスイッチ（ＳＷ＃１２）７１ｂ－１をスイッチし、バッファ群の上位下位ビットに順番にデータを送る経路を確保する（処理Ｃ２－４）。

【０１７３】要求側のボード内スイッチ制御部８２－１は指示された設定を行うと、データを送出する。供給側のボード内スイッチ制御部８２－１は送られてきたデータをバッファＡ群７７－１またはバッファＢ群７８－１で受取る（処理Ｃ２－５）。以後、要求側及び供給側ともに上記の処理Ｃ１－８～Ｃ１－１０を行う（図２７及び図２８参照）。

【０１７４】２５６ビットのデータを２５６ビットポートへ転送する際に帯域を確保できない場合（Ｃ３の場合）、要求側及び供給側ともに上記の処理Ｃ１－１～Ｃ１－３を行う。

【０１７５】その後に、供給側のクロスバスイッチ側アドレス制御部６１－１は識別ビットＳａ，Ｓｂをみてポートａ及びポートｂが使用中であることを認識し、帯域確保不可信号を返答する（処理Ｃ３－１）。

【０１７６】要求側のクロスバスイッチ側アドレス制御部６１－１は帯域確保不可信号をボードにそのまま伝達し、識別ビットＳａ，Ｓｂをともに“０”にする（Ｓａ＝１→０，Ｓｂ＝１→０）（処理Ｃ３－２）。

【０１７７】要求側のボード内アドレス制御部８１－１は従来装置のコントローラ２２－１に帯域確保不可信号をそのまま伝達する（処理Ｃ３－３）。以降、従来装置のコントローラ２２－１の再送要求にまかせる。従来装置における再送のきっかけを受領側が出している場合は、受領側の従来装置のコントローラ２２－１まで要求することで、その方式のまま使用可能である（図２９及び図３０参照）。

【０１７８】１２８ビットのデータを２５６ビットポートへ転送する際に１２８ビット帯域を確保できる場合（Ｃ４の場合）、要求側のクロスバスイッチ側アドレス制御部６１－１は唯一のアドレス線から受領側の２つのアドレス線のいずれかに転送要求を送出する。供給側のクロスバスイッチ側アドレス制御部６１－１は２つのアドレス線のいずれか一方の転送要求を検出する（処理Ｃ４－１）。

【０１７９】供給側のクロスバスイッチ側アドレス制御部６１－１は識別ビットＳａ，Ｓｂをみて少なくともポ

ートａ，ｂいずれかが空いていることを確認し、空いているいずれかのポートのアドレス線から転送ＯＫを返事する側の識別ビットを“１”にする（処理Ｃ４－２）。

【０１８０】要求側のクロスバスイッチ側アドレス制御部６１－１は２つのアドレス線の一方から転送ＯＫを確認すると、ボードに転送ＯＫを伝達し、以降データ送付先を返事のあったポートに変更する。ボード内アドレス制御部８１－１は従来装置のコントローラ２２－１に転送ＯＫをそのまま伝達する（処理Ｃ４－３）。

【０１８１】この後、供給側では上記の処理Ｃ２－２～Ｃ２－５，Ｃ１－８～１－１０を行う。また、要求側では処理Ｃ４－３を行うと、以降、従来装置のコントローラ２２－１からの信号とデータとをそのまま出力する（図３１及び図３２参照）。

【０１８２】１２８ビットのデータを２５６ビットポートへ転送する際に帯域を確保できない場合（Ｃ５の場合）、要求側のクロスバスイッチ側アドレス制御部６１－１は唯一のアドレス線から受領側のいずれかのアドレス線に転送要求を送出する。供給側のクロスバスイッチ側アドレス制御部６１－１は２つのアドレス線の一方の転送要求を検出する（処理Ｃ５－１）。

【０１８３】供給側のクロスバスイッチ側アドレス制御部６１－１は識別ビットＳａ，Ｓｂをみてポートａ及びポートｂが使用中であることを認識し、帯域確保不可信号を返答する（処理Ｃ５－２）。

【０１８４】要求側のクロスバスイッチ側アドレス制御部６１－１は帯域確保不可信号をボードにそのまま伝達する（処理Ｃ５－３）。以降、従来装置のコントローラ２２－１の再送要求にまかせる。従来装置における再送のきっかけを受領側が出している場合は、受領側の従来装置のコントローラ２２－１まで要求することで、その方式のまま使用可能である（図３３及び図３４参照）。

【０１８５】２５６ビットのデータを１２８ビットポートへ転送する際に１２８ビット帯域を確保できる場合（Ｃ６の場合）、要求側のクロスバスイッチ側アドレス制御部６１－１は２つのアドレス線のいずれかに転送要求を送出する。供給側のクロスバスイッチ側アドレス制御部６１－１はアドレス線から転送要求を検出する（処理Ｃ６－１）。

【０１８６】供給側のクロスバスイッチ側アドレス制御部６１－１は送り主のポートにあるアドレス線に転送ＯＫを返事する。要求側のクロスバスイッチ側アドレス制御部６１－１はアドレス線から転送ＯＫを確認すると、ボードに転送ＯＫを伝達する（処理Ｃ６－２）。

【０１８７】この後、要求側では上記の処理Ｃ２－３～Ｃ２－５，Ｃ１－８～１－１０を行う。また、供給側では処理Ｃ６－２を行うと、以降、従来装置のコントローラ２２－１へ信号とデータとをそのまま従来装置に入力する（図３５及び図３６参照）。

【０１８８】２５６ビットのデータを１２８ビットポートへ転送する際に帯域を確保できない場合（Ｃ７の場合）、要求側のクロスバスイッチ側アドレス制御部６１－１は２つのアドレス線のいずれかから転送要求を送出する。供給側のクロスバスイッチ側アドレス制御部６１－１はアドレス線から転送要求を検出する（処理Ｃ７－１）。

【０１８９】供給側のクロスバスイッチ側アドレス制御部６１－１は送り主のポートのあるアドレス線に帯域確保不可信号を返事する。要求側のクロスバスイッチ側アドレス制御部６１－１はアドレス線から帯域確保不可信号を確認すると、帯域確保不可信号をボードに伝達する（処理Ｃ７－２）。

【０１９０】以降、従来装置のコントローラ２２－１の再送要求にまかせる。従来装置における再送のきっかけを受領側が出している場合は、受領側の従来装置のコントローラ２２－１まで要求することで、その方式のまま使用可能である（図３７及び図３８参照）。

【０１９１】このように、幅の広いデータを受けられるボードに２系統の入力バッファとこれにデータを振り分けるスイッチ及びコントローラを持っているので、２つのデータ幅の異なるボードと同時に転送を行うことができる。

【０１９２】また、幅の広いデータを送ることが可能なボードの出力バッファの先にデータを振り分けるスイッチ及びコントローラを持っているので、データを転送中であっても半分のデータ幅に相当するポートが未使用であれば別のデータ転送を行うことができる。

【０１９３】さらに、２組のアドレス線を設ける代わりに１本のアドレス線と２ビットの識別ビットと１ビットのａ，ｂポート識別線とを使用しているので、接続部分の物理的なサイズを小さくし、安価に実現することができる。

【０１９４】さらにまた、データ線／アドレス線ともに通信相手のバス幅に依存せずに共用化を図っているので、通信相手のデータ幅に合わせたポートを複数設けるよりも安価に実現することができる。

【０１９５】

【発明の効果】以上説明したように本発明によれば、複数のボードが夫々接続される同一データ幅の複数のポートを有し、アドレス信号を共有する複数のポートを介して複数のボード間を接続するデータ幅可変型クロスバスイッチ装置において、通信するボード同士のデータ幅が異なる際に、データ幅が広いボードが接続されるポートのうちの空いているポートを介して他のボードとの通信を行うことによって、クロスバスイッチに接続されたデータ幅が広いポートにおいて、データ幅が狭いポートとの通信中にも相手先のポートのデータ幅に関わらず通信することができるという効果がある。

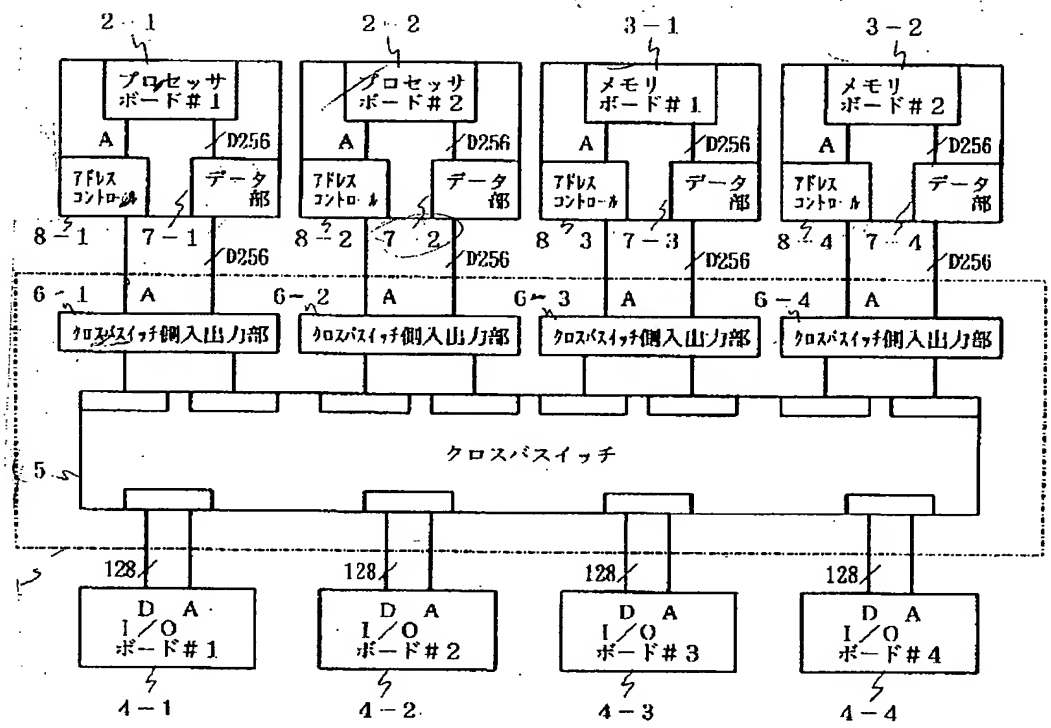
【図面の簡単な説明】

【図１】本発明の一実施例によるクロスバスイッチ装置

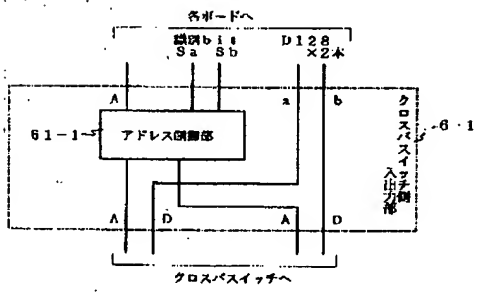
の構成を示すブロック図である。
【図２】図１のクロスバスイッチ側入出力部の構成を示すブロック図である。
【図３】図１のデータ部の構成を示すブロック図である。
【図４】図１のアドレスコントロール部の構成を示すブロック図である。
【図５】図３のボード内スイッチの構成を示すブロック図である。
【図６】（ａ），（ｂ）は図３及び図５に示すスイッチの構成を示す図である。
【図７】図２に示すクロスバスイッチ側アドレス制御部の構成を示すブロック図である。
【図８】（ａ）は図７のメモリ（Ａ）の記憶内容を示す図、（ｂ）は図７のメモリ（Ｂ）の記憶内容を示す図である。
【図９】図４のボード内アドレス制御部の構成を示すブロック図である。
【図１０】（ａ）は図９のメモリ（Ｃ）の記憶内容を示す図、（ｂ）は図９のメモリ（Ｄ）の記憶内容を示す図である。
【図１１】図４のボード内スイッチ制御部による図３及び図５のスイッチの制御を示す図である。
【図１２】図２及び図７に示すクロスバスイッチ側アドレス制御部の動作を示すフローチャートである。
【図１３】図２及び図７に示すクロスバスイッチ側アドレス制御部の動作を示すフローチャートである。
【図１４】図２及び図７に示すクロスバスイッチ側アドレス制御部の動作を示すフローチャートである。
【図１５】図２及び図７に示すクロスバスイッチ側アドレス制御部の動作を示すフローチャートである。
【図１６】図４及び図９に示すボード内アドレス制御部の動作を示すフローチャートである。
【図１７】図４及び図９に示すボード内アドレス制御部の動作を示すフローチャートである。
【図１８】図４及び図９に示すボード内アドレス制御部の動作を示すフローチャートである。
【図１９】図４及び図９に示すボード内アドレス制御部の動作を示すフローチャートである。
【図２０】図４及び図９に示すボード内アドレス制御部の動作を示すフローチャートである。
【図２１】図４及び図９に示すボード内アドレス制御部の動作を示すフローチャートである。
【図２２】図４及び図９に示すボード内アドレス制御部の動作を示すフローチャートである。
【図２３】図４及び図９に示すボード内アドレス制御部の動作を示すフローチャートである。
【図２４】本発明の一実施例によるクロスバスイッチ装置におけるデータ転送の場合分けを示す図である。
【図２５】本発明の一実施例による２５６ビットのデータを２５６ビットポートへ転送する際に２５６ビット帯域を確保できる場合の要求側の動作を示す図である。
【図２６】本発明の一実施例による２５６ビットのデータを２５６ビットポートへ転送する際に２５６ビット帯域を確保できる場合の供給側の動作を示す図である。
【図２７】本発明の一実施例による２５６ビットのデータを２５６ビットポートへ転送する際に１２８ビット帯域を確保できる場合の要求側の動作を示す図である。
【図２８】本発明の一実施例による２５６ビットのデータを２５６ビットポートへ転送する際に１２８ビット帯域を確保できる場合の供給側の動作を示す図である。
【図２９】本発明の一実施例による２５６ビットのデータを２５６ビットポートへ転送する際に帯域を確保できない場合の要求側の動作を示す図である。
【図３０】本発明の一実施例による２５６ビットのデータを２５６ビットポートへ転送する際に帯域を確保できない場合の供給側の動作を示す図である。
【図３１】本発明の一実施例による１２８ビットのデータを２５６ビットポートへ転送する際に１２８ビット帯域を確保できる場合の要求側の動作を示す図である。
【図３２】本発明の一実施例による１２８ビットのデータを２５６ビットポートへ転送する際に１２８ビット帯域を確保できる場合の供給側の動作を示す図である。
【図３３】本発明の一実施例による１２８ビットのデータを２５６ビットポートへ転送する際に帯域を確保できない場合の要求側の動作を示す図である。
【図３４】本発明の一実施例による１２８ビットのデータを２５６ビットポートへ転送する際に帯域を確保できない場合の供給側の動作を示す図である。
【図３５】本発明の一実施例による２５６ビットのデータを１２８ビットポートへ転送する際に１２８ビット帯域を確保できる場合の要求側の動作を示す図である。
【図３６】本発明の一実施例による２５６ビットのデータを１２８ビットポートへ転送する際に１２８ビット帯域を確保できる場合の供給側の動作を示す図である。
【図３７】本発明の一実施例による２５６ビットのデータを１２８ビットポートへ転送する際に帯域を確保できない場合の要求側の動作を示す図である。
【図３８】本発明の一実施例による２５６ビットのデータを１２８ビットポートへ転送する際に帯域を確保できない場合の供給側の動作を示す図である。
【図３９】従来例によるクロスバスイッチ装置の構成を示すブロック図である。
【図４０】図３９のプロセッサボードの構成を示すブロック図である。
【符号の説明】
１　クロスバスイッチ装置
２－１，２－２　プロセッサボード
３－１，３－２　メモリボード
４－１～４－４　Ｉ／Ｏボード

5　クロスバスイッチ
6－1～6－4　クロスバスイッチ側入出力部
7－1～7－4　データ部
8－1～8－4　アドレスコントロール部
61－1　クロスバスイッチ側アドレス制御部
61a－1　コントローラ
61b－1　メモリ（A）
61c－1　メモリ（B）
71－1　ボード内スイッチ
72－1，73－1　バッファ
74－1～76－1，
71a－1～71j－1　スイッチ
77－1　バッファA群
78－1　バッファB群
81－1　ボード内アドレス制御部
81a－1　コントローラ
81b－1　メモリ（C）
81c－1　メモリ（D）
81d－1～81g－1　カウンタ
82－1　ボード内スイッチ制御部

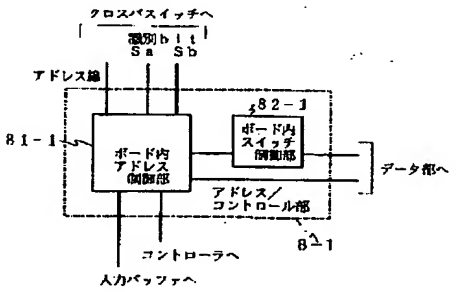
【図1】



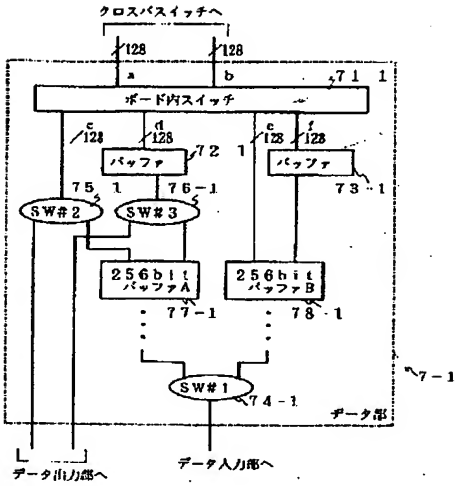
【図2】



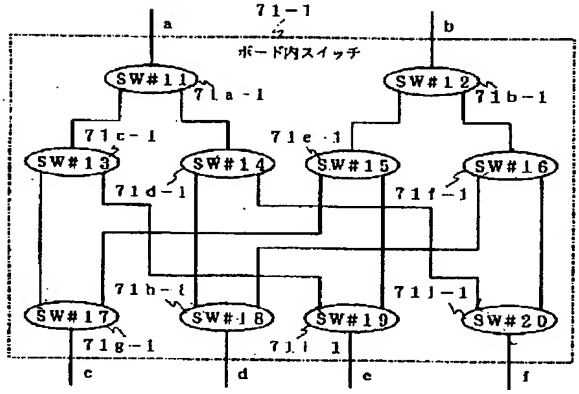
【図4】



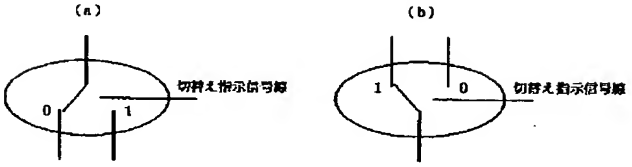
【図3】



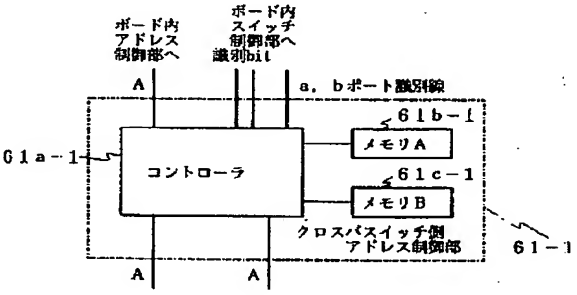
【図5】



【図6】



【図7】



【図8】

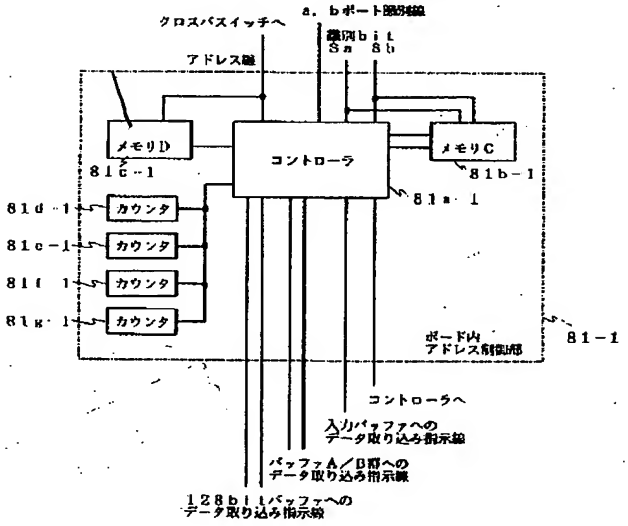
(a)

ボード名	ポート名
プロセッサ#1	a b
プロセッサ#2	a b
メモリ#1	a b
メモリ#2	a b
I／O#1	a
I／O#2	a
I／O#3	a
I／O#4	a

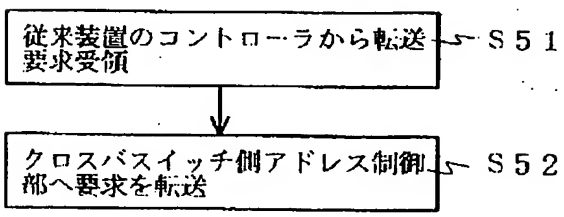
(b)

aポート の通信 相手先 ボード名	aポート の通信 相手先 ポート名
bポート の通信 相手先 ボード名	bポート の通信 相手先 ポート名

【図9】



【図16】



【図10】

（a）

現在のSaの値	現在のSbの値
1クロック前のSaの値	1クロック前のSbの値

（b）

バッファA群用		バッファB群用	
AA1	NAA1	AB1	NAB1
AA2	NAA2	AB2	NAB2
AA3	NAA3	AB3	NAB3
AA4	NAA4	AB4	NAB4
・	・	・	・
・	・	・	・
・	・	・	・
・	・	・	・
・	・	・	・

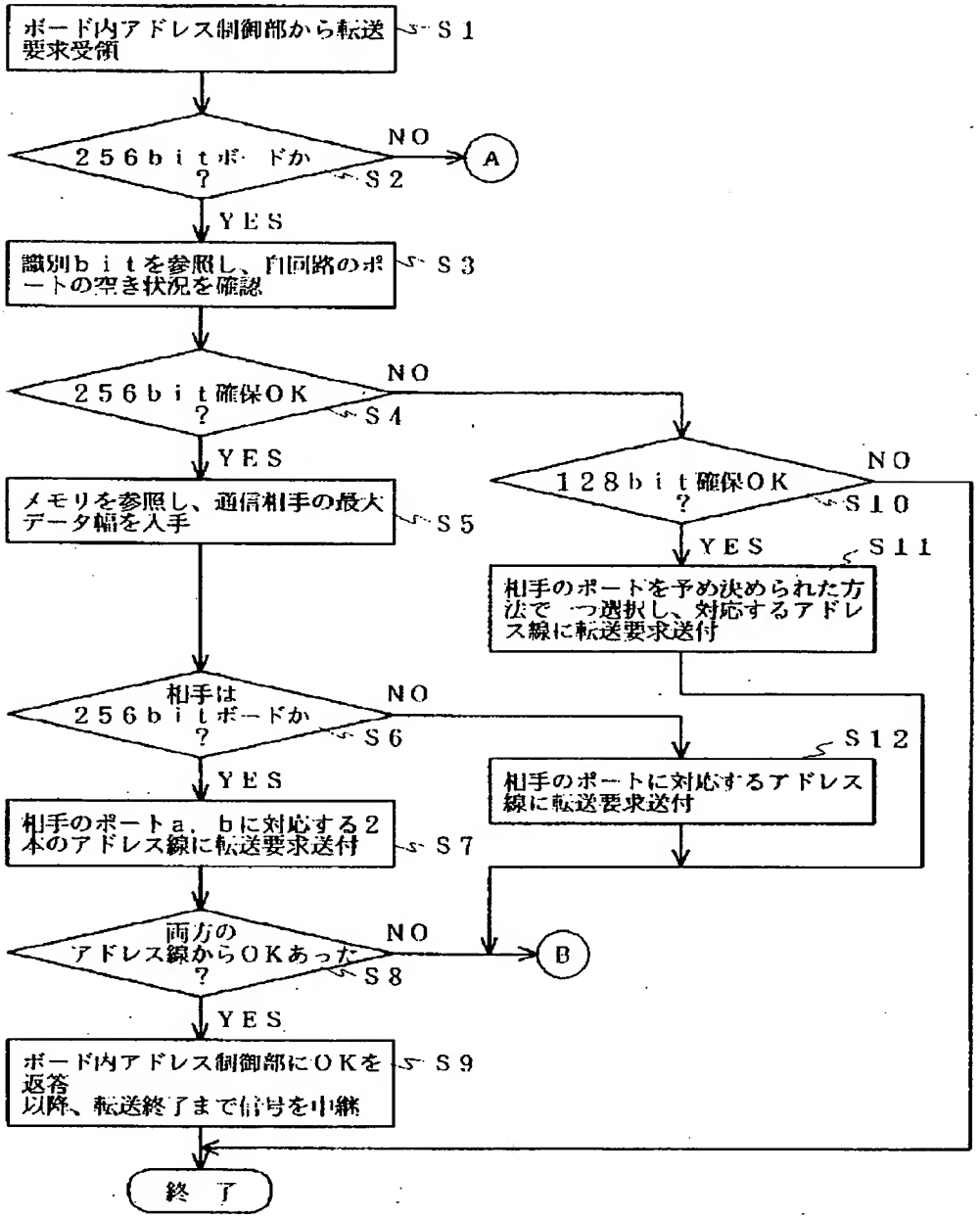
【図24】

256bit→256bitポートへ	256bit帯域確保OK	C1
	128bit帯域確保OK	C2
	帯域確保不可	C3
128bit→256bitポートへ	128bit以上帯域確保OK	C4
	帯域確保不可	C5
256bit→128bitポートへ	128bit帯域確保OK	C6
	帯域確保不可	C7
128bit→128bitポートへ	128bit帯域確保OK	C8
	帯域確保不可	C9

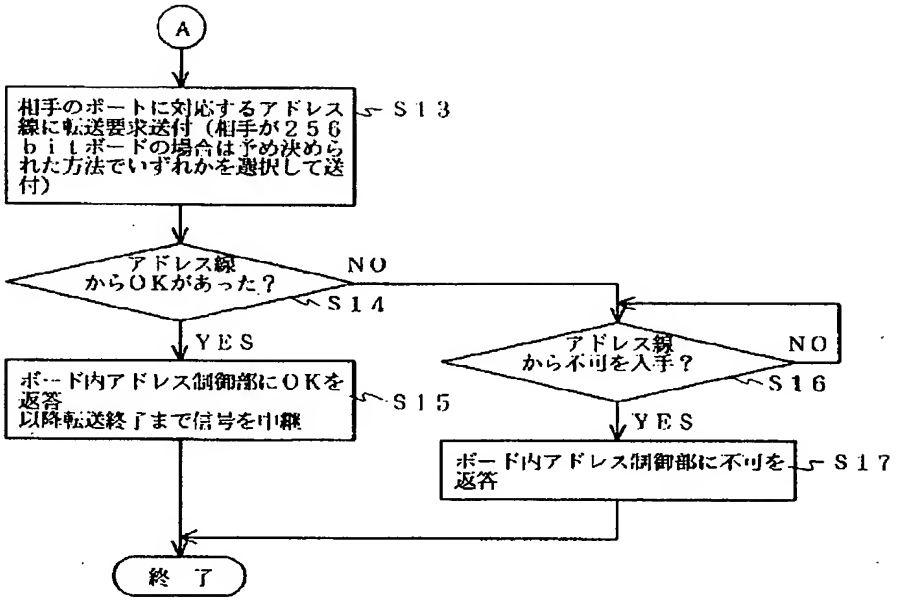
【図11】

	SW#1	SW#2	SW#3	SW#11	SW#12	SW#13	SW#14	SW#15	SW#16	SW#17	SW#18	SW#19	SW#20
a→c b→d	−	−	−	0	1	0	−	−	0	1	0	−	−
a→e b→f	−	0	0	0	1	1	−	−	1	−	−	1	0
a→c, d	−	0	0	1 0	−	− 0	0 −	−	−	− 1	1 −	−	−
a→c, f	−	0	0	1 0	−	− 1	1 −	−	−	−	−	− 1	1 −
b→c, d	−	0	0	−	1 0	−	−	− 0	0 −	− 0	0 −	−	−
b→c, f	−	0	0	−	1 0	−	−	− 1	1 −	−	−	− 0	0 −
c, d→a	−	1	1	0 1	−	0 −	− 0	−	−	1 −	− 1	−	−
c, d→b	−	1	1	−	0 1	−	−	0 −	− 0	−	−	0 −	− 0
出力側へ	−	0	0	−	−	−	−	−	−	−	−	−	−
入力側へ	−	1	1	−	−	−	−	−	−	−	−	−	−
A群出力	1	−	−	−	−	−	−	−	−	−	−	−	−
B群出力	0	−	−	−	−	−	−	−	−	−	−	−	−

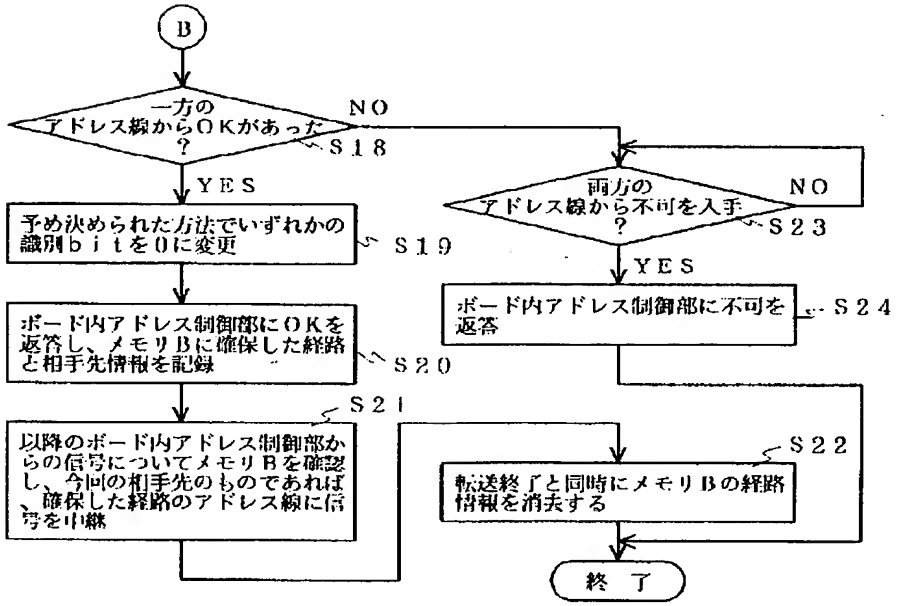
【図12】


ボード内アドレス制御部から転送要求受領
S1
256bitボードか？
NO
A
S2
YES
識別bitを参照し、自回路のポートの空き状況を確認
S3
256bit確保OK？
NO
S4
YES
メモリを参照し、通信相手の最大データ幅を入手
S5
128bit確保OK？
NO
S10
YES
S11
相手のポートを予め決められた方法で一つ選択し、対応するアドレス線に転送要求送付
相手は256bitボードか？
NO
S6
S12
相手のポートに対応するアドレス線に転送要求送付
YES
相手のポートa，bに対応する2本のアドレス線に転送要求送付
S7
両方のアドレス線からOKあった？
NO
B
S8
YES
ボード内アドレス制御部にOKを返答
以降、転送終了まで信号を中継
S9
終了

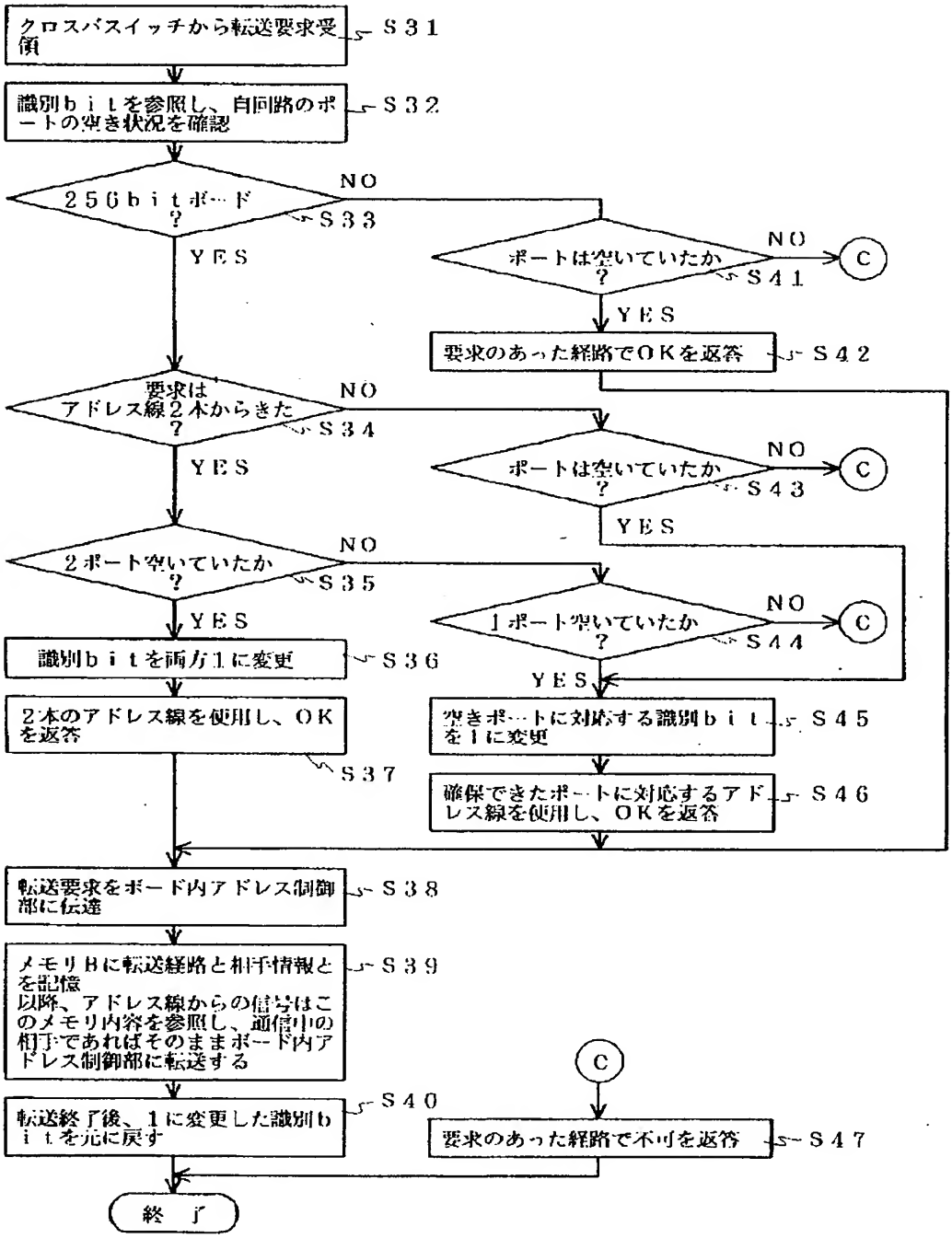
【図１３】


A
相手のポートに対応するアドレス線に転送要求送付（相手が２５６ｂｉｔボードの場合は予め決められた方法でいずれかを選択して送付）
Ｓ１３
アドレス線からＯＫがあった？
ＮＯ
Ｓ１４
ＹＥＳ
ボード内アドレス制御部にＯＫを返答以降転送終了まで信号を中継
Ｓ１５
アドレス線から不可を入手？
ＮＯ
Ｓ１６
ＹＥＳ
ボード内アドレス制御部に不可を返答
Ｓ１７
終　了

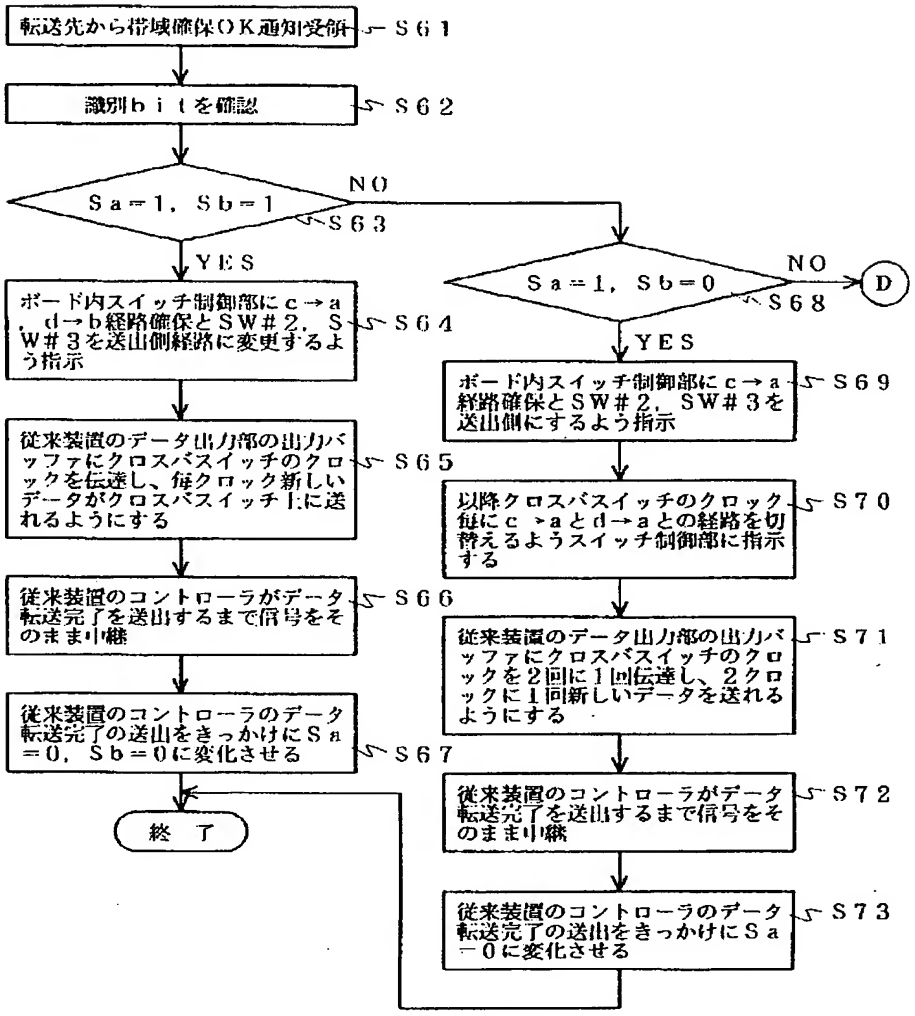
【図１４】


B
一方のアドレス線からＯＫがあった？
ＮＯ
Ｓ１８
ＹＥＳ
予め決められた方法でいずれかの識別ｂｉｔを０に変更
Ｓ１９
ボード内アドレス制御部にＯＫを返答し、メモリＢに確保した経路と相手先情報を記録
Ｓ２０
Ｓ２１
以降のボード内アドレス制御部からの信号についてメモリＢを確認し、今回の相手先のものであれば、確保した経路のアドレス線に信号を中継
両方のアドレス線から不可を入手？
ＮＯ
Ｓ２３
ＹＥＳ
ボード内アドレス制御部に不可を返答
Ｓ２４
Ｓ２２
転送終了と同時にメモリＢの経路情報を消去する
終　了

【図15】


クロスバスイッチから転送要求受領
S31
識別ｂｉｔを参照し、自回路のポートの空き状況を確認
S32
256ｂｉｔボード？
S33
NO
YES
ポートは空いていたか？
S41
NO
C
YES
要求のあった経路でＯＫを返答
S42
要求はアドレス線2本からきた？
S34
NO
YES
ポートは空いていたか？
S43
NO
C
YES
2ポート空いていたか？
S35
NO
YES
1ポート空いていたか？
S44
NO
C
YES
識別ｂｉｔを両方1に変更
S36
2本のアドレス線を使用し、ＯＫを返答
S37
空きポートに対応する識別ｂｉｔを1に変更
S45
確保できたポートに対応するアドレス線を使用し、ＯＫを返答
S46
転送要求をボード内アドレス制御部に伝達
S38
メモリBに転送経路と相手情報とを記憶
以降、アドレス線からの信号はこのメモリ内容を参照し、通信中の相手であればそのままボード内アドレス制御部に転送する
S39
転送終了後、1に変更した識別ｂｉｔを元に戻す
S40
C
要求のあった経路で不可を返答
S47
終了

【図１７】



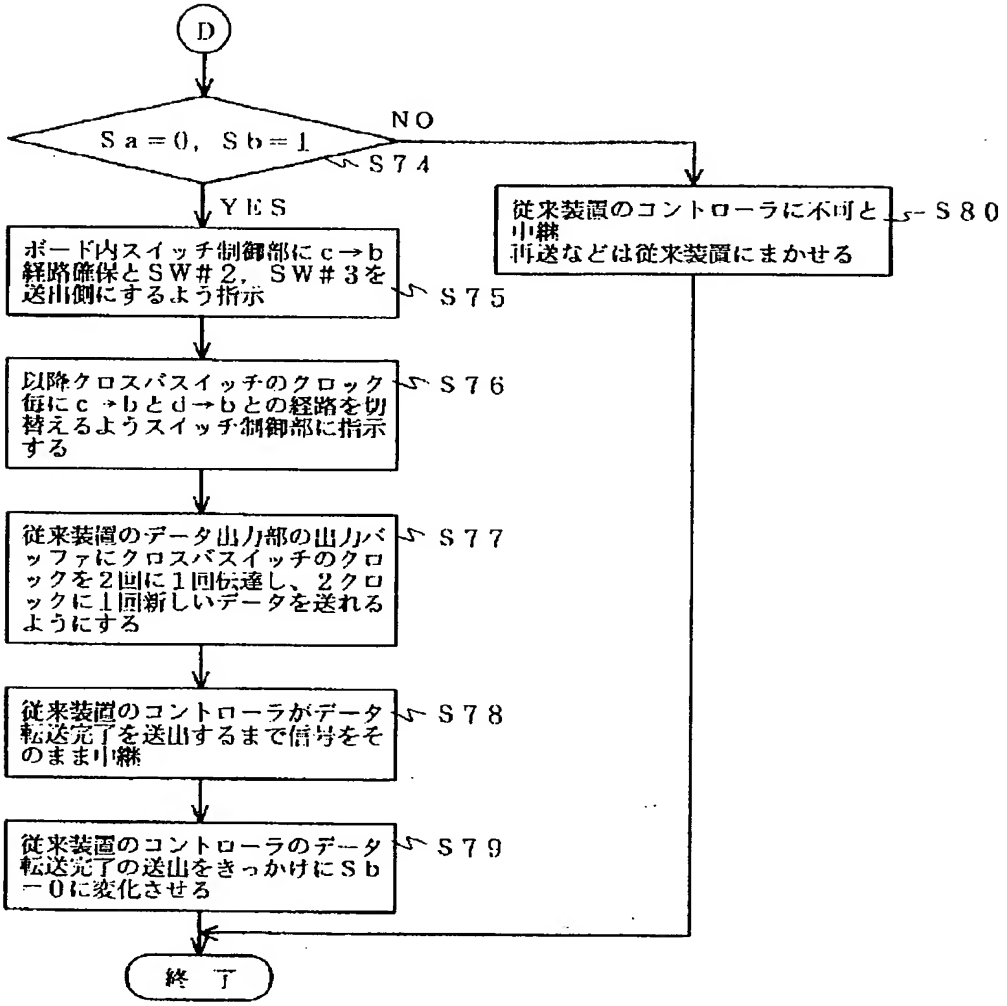
【図３１】

	要求側			
	ボード内アドレス制御部	ボード内スイッチ制御部	クロスバスイッチ側アドレス制御部	識別ｂｉｔ
Ｃ４－１			唯一のアドレス線から受信側のいずれかのアドレス線へ要求送出	無し
Ｃ４－２				無し
Ｃ４－３	従来装置のコントローラに信号をそのまま伝達		信号をボード側にそのまま伝達 以降、データ送付先を返事のあったポートに変更	無し
以降、従来装置のコントローラからの信号とデータとをそのまま出力				無し

【図３３】

	要求側			
	ボード内アドレス制御部	ボード内スイッチ制御部	クロスバスイッチ側アドレス制御部	識別ｂｉｔ
Ｃ５－１	無し	無し	唯一のアドレス線から受信側のいずれかのアドレス線へ要求送出	無し
Ｃ５－２	無し	無し		無し
Ｃ５－３	無し	無し	不明の信号をボード側にそのまま伝達	無し
以降、従来装置のコントローラの再送要求にまかせる 従来装置における再送のきっかけを受信側が出している場合は、受信側の従来装置のコントローラまで要求を出すことで、その方式のまま動作可能。				

【図１８】



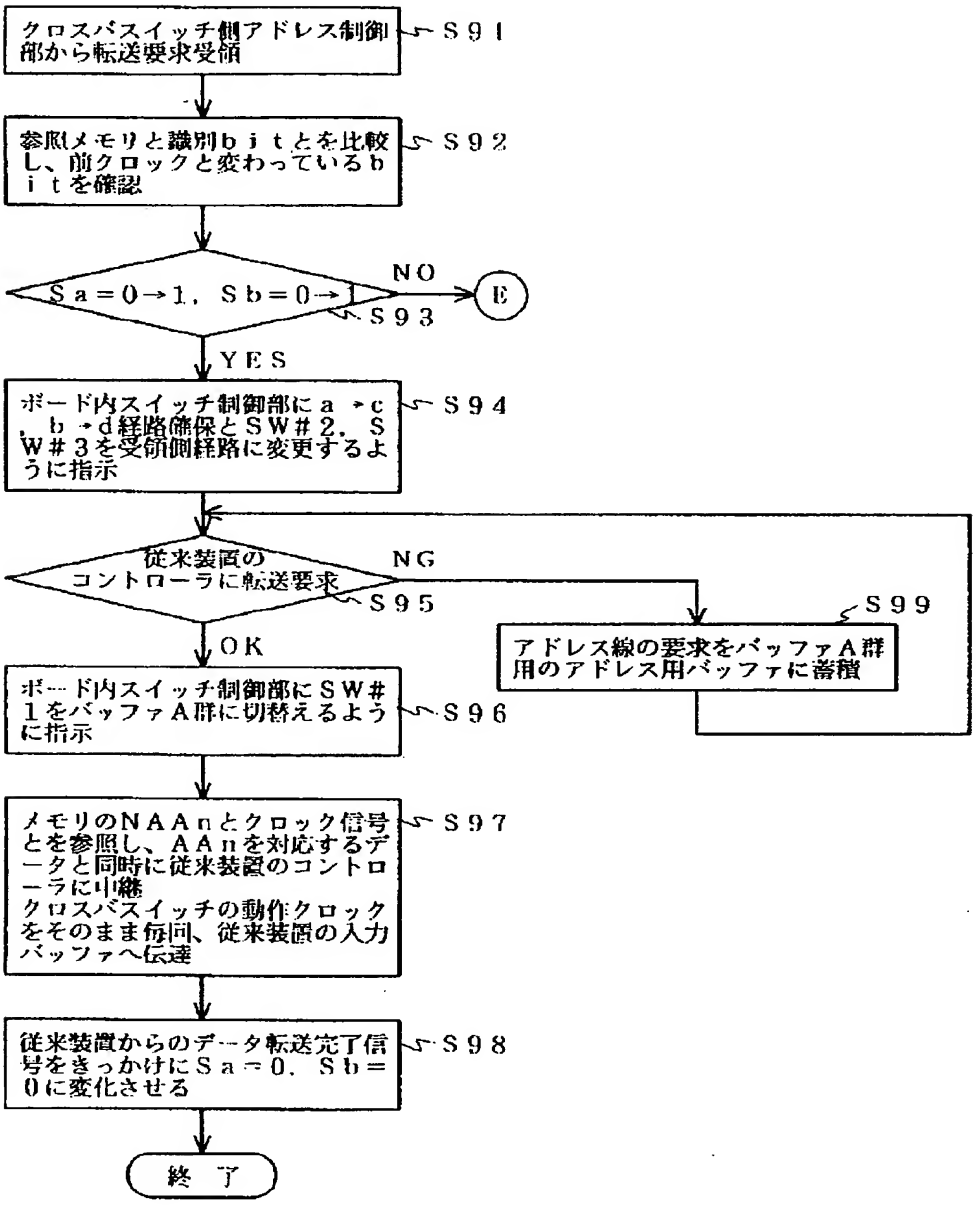
【図３４】

	供給側			
	クロスバスイッチ側アドレス制御部	ボード内アドレス制御部	ボード内スイッチ制御部	識別ｂｉｔ
Ｃ５－１	一方のアドレス線の要求を検出			1，1
Ｃ５－２	識別ｂｉｔをみて、ａ，ｂが使用中であることを認識し、帯域確保不可信号を返送			1，1
Ｃ５－３				
以降、従来装置のコントローラの再送要求にまかせる 従来装置における再送のきっかけを受領側が出している場合は、 受領側の従来装置のコントローラまで要求を出すことで、 その方式のまま使用可能。				

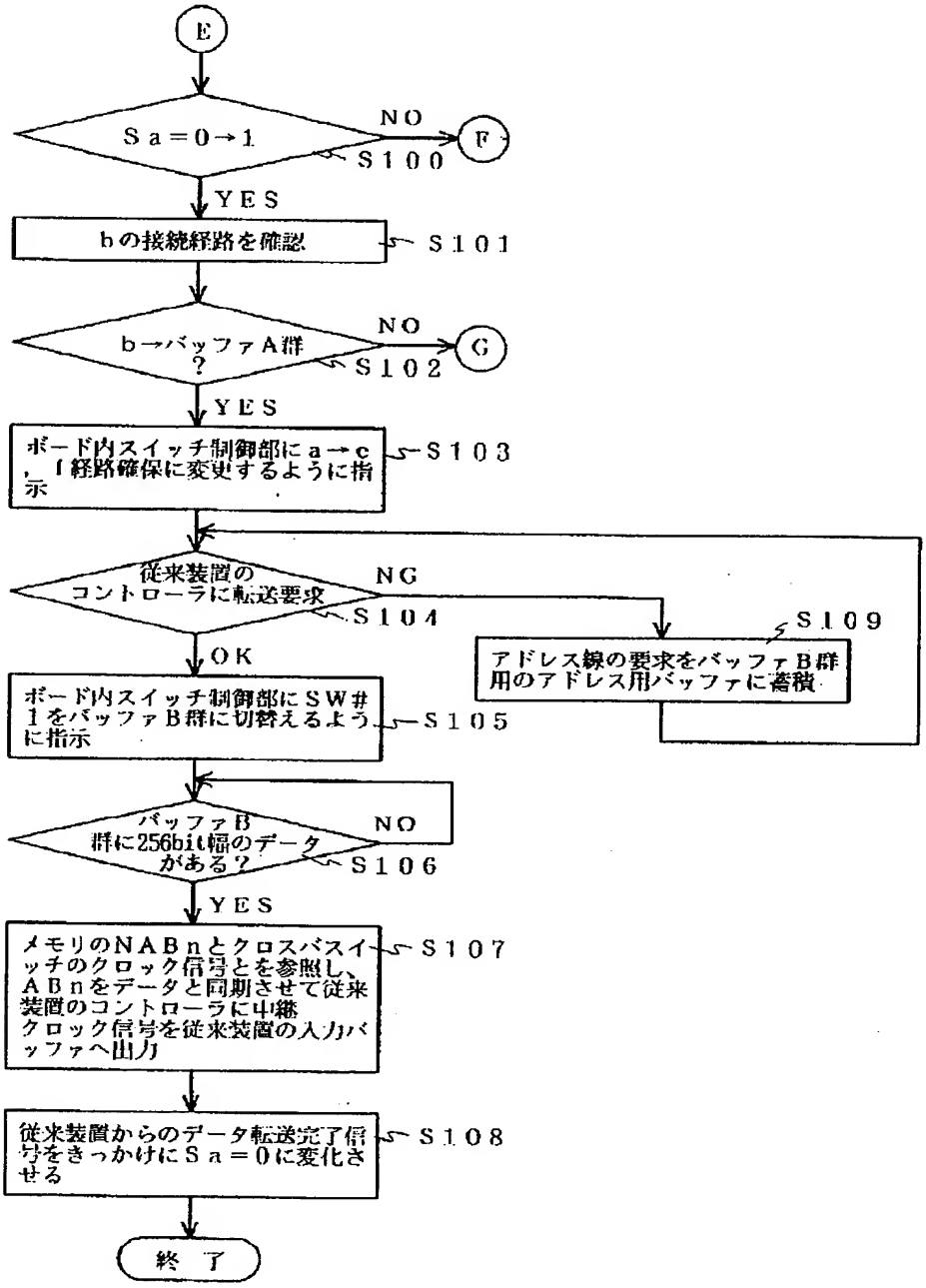
【図３７】

	要求側			
	ボード内アドレス制御部	ボード内スイッチ制御部	クロスバスイッチ側アドレス制御部	識別ｂｉｔ
Ｃ７－１			いずれかのアドレス線から要求送出	０→１，？ or ２，０→１
Ｃ７－２			アドレス線から不可を確認 ボードに不可と伝達	
以降、従来装置のコントローラの再送要求にまかせる 従来装置における再送のきっかけを受領側が出している場合は、 受領側の従来装置のコントローラまで要求を出すことで、 その方式のまま使用可能。				

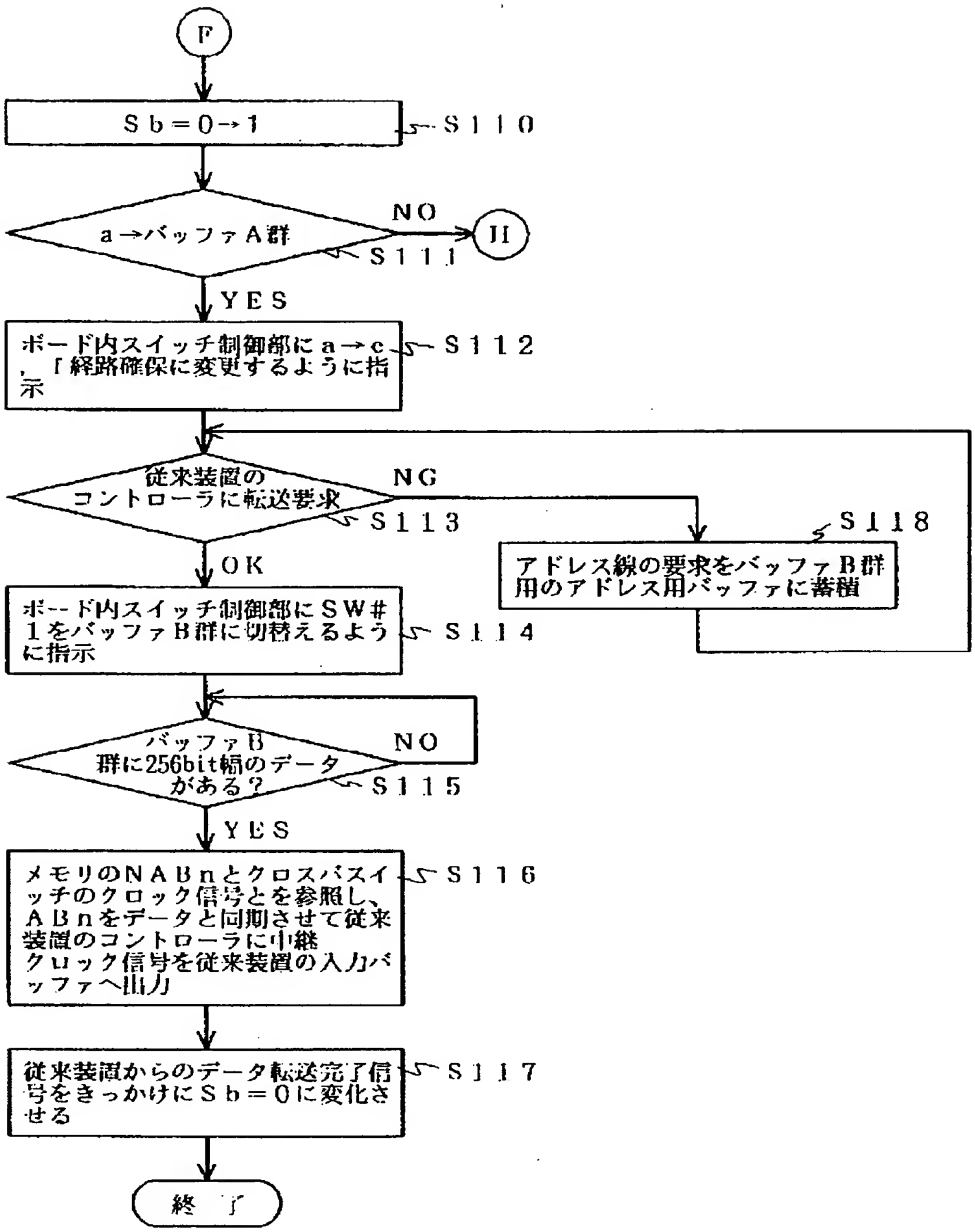
【図19】


クロスバスイッチ側アドレス制御部から転送要求受領
S91
参照メモリと識別ｂｉｔとを比較し、前クロックと変わっているｂｉｔを確認
S92
Sa＝0→1，Sb＝0→1
S93
NO
E
YES
ボード内スイッチ制御部にａ→ｃ，ｂ→ｄ経路確保とSW#2，SW#3を受領側経路に変更するように指示
S94
従来装置のコントローラに転送要求
S95
NG
S99
アドレス線の要求をバッファA群用のアドレス用バッファに蓄積
OK
ボード内スイッチ制御部にSW#1をバッファA群に切替えるように指示
S96
メモリのNAAnとクロック信号とを参照し、AAnを対応するデータと同時に従来装置のコントローラに中継
クロスバスイッチの動作クロックをそのまま毎回、従来装置の入力バッファへ伝達
S97
従来装置からのデータ転送完了信号をきっかけにSa＝0，Sb＝0に変化させる
S98
終了

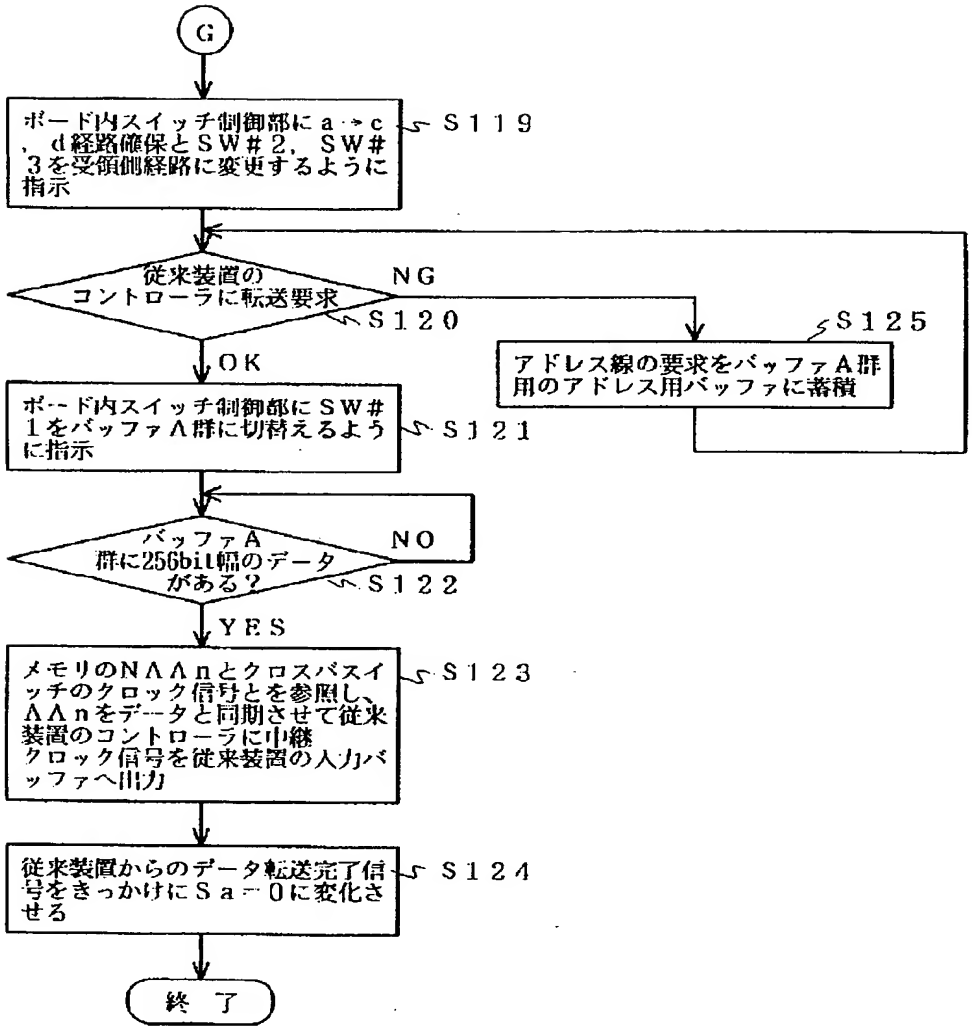
【図２０】


E
Ｓａ＝０→１
NO
Ｓ１００
F
YES
ｂの接続経路を確認
Ｓ１０１
ｂ→バッファＡ群？
NO
Ｓ１０２
G
YES
ボード内スイッチ制御部にａ→ｃ，「経路確保に変更するように指示
Ｓ１０３
従来装置のコントローラに転送要求
NG
Ｓ１０４
Ｓ１０９
アドレス線の要求をバッファＢ群用のアドレス用バッファに蓄積
OK
ボード内スイッチ制御部にＳＷ#１をバッファＢ群に切替えるように指示
Ｓ１０５
バッファＢ群に256bit幅のデータがある？
NO
Ｓ１０６
YES
メモリのＮＡＢｎとクロスバスイッチのクロック信号とを参照し、ＡＢｎをデータと同期させて従来装置のコントローラに中継
クロック信号を従来装置の入力バッファへ出力
Ｓ１０７
従来装置からのデータ転送完了信号をきっかけにＳａ＝０に変化させる
Ｓ１０８
終　了

【図２１】


F
Ｓｂ＝０→１
Ｓ１１０
ａ→バッファＡ群
NO
Ｓ１１１
JJ
YES
ボード内スイッチ制御部にａ→ｃ，「経路確保に変更するように指示
Ｓ１１２
従来装置のコントローラに転送要求
NG
Ｓ１１３
Ｓ１１８
アドレス線の要求をバッファＢ群用のアドレス用バッファに蓄積
OK
ボード内スイッチ制御部にＳＷ＃１をバッファＢ群に切替えるように指示
Ｓ１１４
バッファＢ群に256bit幅のデータがある？
NO
Ｓ１１５
YES
メモリのＮＡＢｎとクロスバスイッチのクロック信号とを参照し、ＡＢｎをデータと同期させて従来装置のコントローラに中継クロック信号を従来装置の入力バッファへ出力
Ｓ１１６
従来装置からのデータ転送完了信号をきっかけにＳｂ＝０に変化させる
Ｓ１１７
終　了

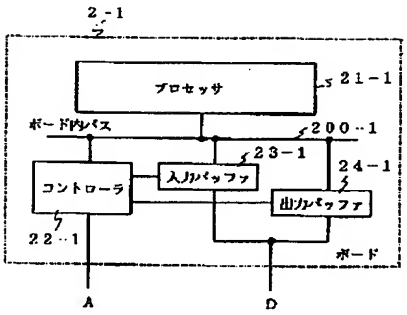
【図２２】



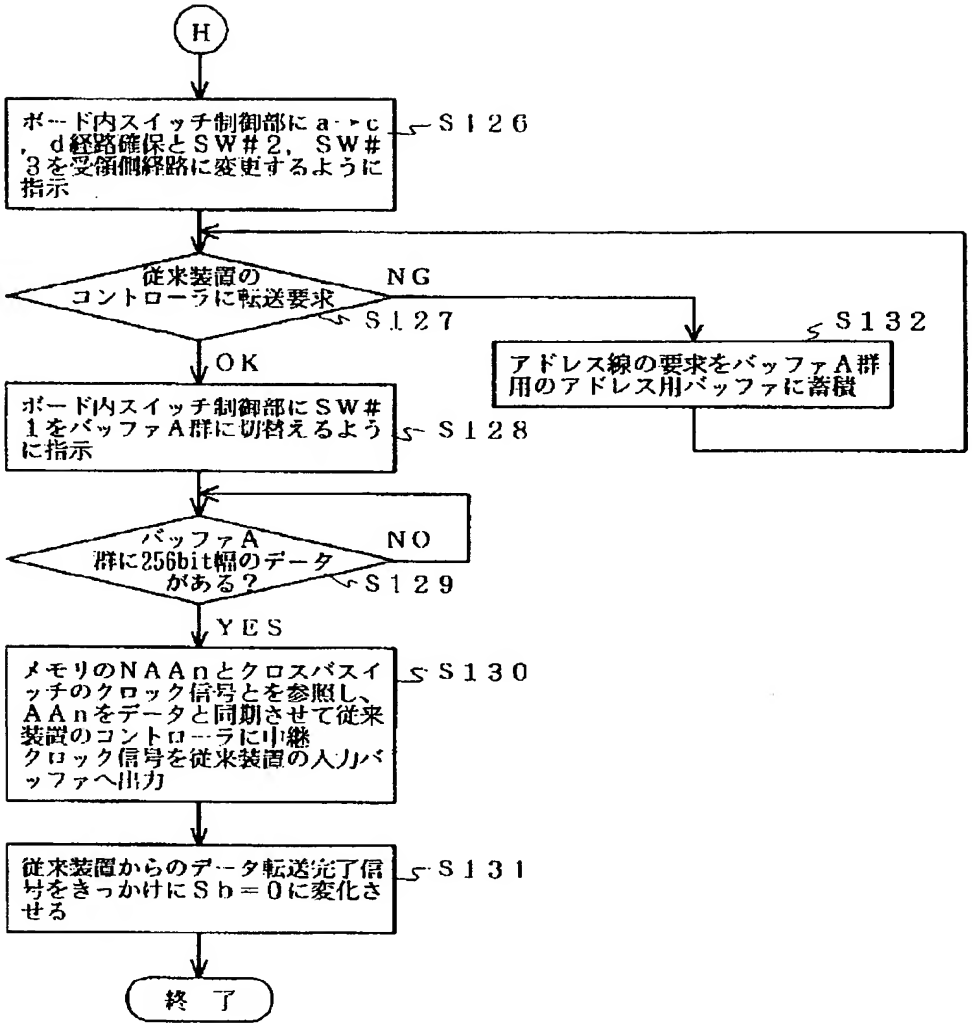
【図３６】

	供給側			
	クロスバスイッチ側アドレス制御部	ボード内アドレス制御部	ボード内スイッチ制御部	識別ｂｉｔ
Ｃ６－１	アドレス線から要求を検出	無し	無し	無し
Ｃ６－２	送り主のポートにあるアドレス線へＯＫを返事	無し	無し	無し
	以降、従来装置のコントローラへの信号とデータとをそのまま従来装置に入力			

【図４０】



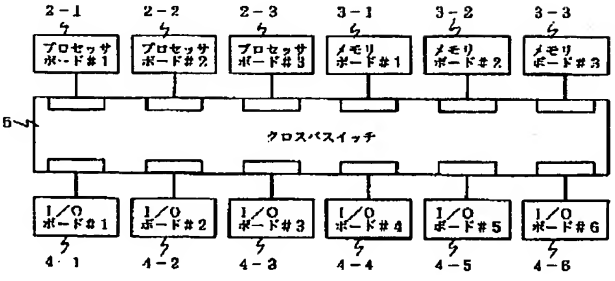
【図23】



【図38】

	供給側			
	クロスバスイッチ側アドレス制御部	ボード内アドレス制御部	ボード内スイッチ制御部	識別bit
C7-1	アドレス線から要求を検出	無し	無し	無し
C7-2	送り先のポートのあるアドレス線へ不可を通事	無し	無し	無し
以降、従来装置のコントローラの再送要求にまかせる 従来装置における再送のきっかけを受領側が出している場合は、 受領側の従来装置のコントローラまで要求を出すことで、 その方式のまま使用可能。				

【図39】



【図25】

	要求側			
	ボード内アドレス制御部	ボード内スイッチ制御部	クロスバスイッチ側アドレス制御部	識別ｂｉｔ
Ｃ１－１	従来装置のコントローラより転送要求あり			０，０
Ｃ１－２	識別ｂｉｔ両方１へ転送要求送出			０→１，０→１
Ｃ１　３			識別ｂｉｔが両方１をみて、通信相手の２つのアドレス線に要求送出	１，１
Ｃ１－４				
Ｃ１－５			両方のアドレス線からＯＫを確認識別ｂｉｔを両方立たせたままボードにＯＫ伝達	１，１
Ｃ１－６	スイッチ制御部へａ→ｃ，ｂ→ｄの経路設定を指示ＳＷ＃２，＃３を送出側へ			１，１
Ｃ１－７		データ送出		１，１
Ｃ１－８				
Ｃ１－９				
Ｃ１－１０	送出完了後識別ｂｉｔを０に			１→０，１→０

【図26】

	供給側			
	クロスバスイッチ側アドレス制御部	ボード内アドレス制御部	ボード内スイッチ制御部	識別ｂｉｔ
Ｃ１－１				０，０
Ｃ１－２				０，０
Ｃ１－３	２つのアドレス線の要求を検出			０，０
Ｃ１－４	識別ｂｉｔ－０をみて、両方のアドレス線にＯＫを返答同時に識別ｂｉｔを立て、要求をボードに伝達	スイッチ制御部へａ→ｃ，ｂ→ｄの経路設定を指示		０→１，０→１
Ｃ１－５		従来装置のコントローラに伝達		１，１
Ｃ１－６				１，１
Ｃ１－７			バッファＡ群データ受け取り	１，１
Ｃ１－８		バッファ群から従来装置のデータ入力中が取り込み中のデータがないか、または取り込み終了を確認		
Ｃ１－９	ＳＷ＃１をバッファＡ群へ	アドレスを従来装置のコントローラに送付		
Ｃ１－１０		転送完了後識別ｂｉｔを０に戻す		１→０，１→０

【図29】

	要求側			
	ボード内アドレス制御部	ボード内スイッチ制御部	クロスバスイッチ側アドレス制御部	識別ｂｉｔ
Ｃ１－１	従来装置のコントローラより転送要求あり			０，０
Ｃ１－２	識別ｂｉｔ両方１へ転送要求送出			０→１，０→１
Ｃ１－３			識別ｂｉｔが両方１をみて、通信相手の２つのアドレス線に要求送出	１，１
Ｃ３－１				
Ｃ３　２			不可の信号をボード側にそのまま伝達識別ｂｉｔを０，０へ	１→０，１→０
Ｃ３－３	従来装置のコントローラに不可信号をそのまま伝達			０，０
以降、従来装置のコントローラの再送要求にまかせる 従来装置における再送のきっかけを受領側が出している場合は、受領側の従来装置のコントローラまで要求することで、その方式のまま使用可能。				

【図30】

	供給側			
	クロスバスイッチ側アドレス制御部	ボード内アドレス制御部	ボード内スイッチ制御部	識別ｂｉｔ
Ｃ１－１				０，０
Ｃ１－２				０，０
Ｃ１　３	２つのアドレス線の要求を検出			１，１
Ｃ３－１	識別ｂｉｔをみて、ａ，ｂが使用中であることを認識し、指域確保不可信号をアドレス線に返答			１，１
Ｃ３　２				１，１
Ｃ３－３				１，１
以降、従来装置のコントローラの再送要求にまかせる 従来装置における再送のきっかけを受領側が出している場合は、受領側の従来装置のコントローラまで要求することで、その方式のまま使用可能。				

【図２７】

	要求側			
	ボード内 アドレス制御部	ボード内 スイッチ制御部	クロスバスイッチ側 アドレス制御部	識別ｂｉｔ
Ｃ１－１	従来装置のコントローラより 転送要求あり			０．０
Ｃ１－２	識別ｂｉｔ 両方１へ 転送要求送出			０→１．０→１
Ｃ１－３			識別ｂｉｔが両方１をみて、送信相手の２つのアドレス部に要求送出	１．１
Ｃ２－１				１．１
Ｃ２　２			一方のアドレス部からＯＫを確認 ＯＫがこなかった方の識別ｂｉｔを０ににし ボードに転送ＯＫを伝達	１．１→０ ｏｒ１→０．１
Ｃ２　３	従来装置のコントローラに転送ＯＫと伝達 ＳＷ＃２，＃３を送出側へ			１．？ ｏｒ？．１
Ｃ２－４	スイッチ制御部へ ｃ→ａｏｒｂ，ｄ→ａｏｒｂを指示 従来装置の出力部に新データを２クロックに１回要求			１．？ ｏｒ？．１
Ｃ２　５		データ送出		１．？ ｏｒ？．１
Ｃ１－８				
Ｃ１－９				
Ｃ１－１０	送出完了後識別ｂｉｔを０に戻す			１→０．１→０

【図２８】

	受信側			
	クロスバスイッチ側 アドレス制御部	ボード内 アドレス制御部	ボード内 スイッチ制御部	識別ｂｉｔ
Ｃ１－１				０．０
Ｃ１－２				０．０
Ｃ１－３	２つのアドレス系の要求を検出			１．０ ｏｒ０．１
Ｃ２－１	識別ｂｉｔをみて、ａまたはｂが使用中であることを認識し、空いている側のアドレス線にＯＫを返答、同時に識別ｂｉｔを立て、要求をボードに伝達			０→１．０→１
Ｃ２－２			スイッチへ接続したポートから被保可能バッファ群へ経路確保を指示	
Ｃ２－３				
Ｃ２－４		従来装置のコントローラに伝達	クロック毎にＳＷ＃１１またはＳＷ＃１２をスイッチし、バッファ群の上位下位ｂｉｔに順番にデータを送る経路を確保	１．１ １．１
Ｃ２－５		バッファＡｏｒＢ群データ受け取り		
Ｃ１－８		バッファ群から従来装置のデータ入力端が取り込み中のデータがないか、または取り込み終了を確認		
Ｃ１－９	ＳＷ＃１をバッファＡ群へ	アドレスを従来装置のコントローラに送付		
Ｃ１－１０		転送完了後識別ｂｉｔを０に戻す		１→０．１→０

【図３２】

	供給側			
	クロスバスイッチ側アドレス設定部	ボード内アドレス制御部	ボード内スイッチ制御部	識別ｂｉｔ
Ｃ４－１	一方のアドレス線の要求を設ける			０，？ ｏｒ？，０
Ｃ４－２	識別ｂｉｔをみて、少なくともａ，ｂいずれか空いていることを確認し、空いているいずれかのポートのアドレス線からＯＫを返答する側の識別ｂｉｔを１にする			０→１，？ ｏｒ？，０→１
Ｃ２－２			スイッチへ接続したポートから確保可能バッファ群へ経路接続を指示	
Ｃ２－３				
Ｃ２－４		従来装置のコントローラに伝達	クロック部にＳＷ＃１１またはＳＷ＃１２をスイッチし、バッファ群の上位下位ｂｉｔに順番にデータを送る経路を確保	１，１ １，１
Ｃ２－５		バッファＡｏｒＢ群データ受け取り		
Ｃ３－８		バッファ群から従来装置のデータ入力部が取り込み中のデータがないか、または取り込み終了を確認		
Ｃ１－９	ＳＷ＃１をバッファＡ群へ	アドレスを従来装置のコントローラに送付		
Ｃ１－１０		転送完了後識別ｂｉｔを０に戻す		１→０，１→０

【図35】

	要求側			
	ボード内 アドレス制御部	ボード内 スイッチ制御部	クロスバスイッチ側 アドレス制御部	識別ｂｉｔ
Ｃ6－1			いずれかのアドレス線から要求送出	0→1，？ ｏｒ？，0→1
Ｃ6－2			アドレス線からＯＫを確認 ボードにＯＫ伝達	
Ｃ2－3	従来装置のコントローラに転送ＯＫと伝達 ＳＷ＃2，＃3を送出側へ			1，？ ｏｒ？，1
Ｃ2－4	スイッチ制御部へ ｃ→ａｏｒｂ， ｄ→ａｏｒｂ を指示 従来装置の出力部に新データを2クロックに1回要求			1，？ ｏｒ？，1
Ｃ2－5	データ送出			1，？ ｏｒ？，1
Ｃ1－8				
Ｃ1－9				
Ｃ1－10	送出完了後識別ｂｉｔを0に戻す			1→0，1→0

PN - JP11296473 A 19991029

PD - 1999-10-29

PR - JP19980103232 19980415

OPD - 1998-04-15

TI - DATA WIDTH VARIABLE TYPE CROSSBAR SWITCHING DEVICE, CONNECTION METHOD THEREFOR, AND MEDIUM FOR STORING CONTROL PROGRAM FOR THE DEVICE

IN - YOKOYAMA ATSUSHI

PA - NIPPON ELECTRIC CO

IC - G06F13/36 ; G06F13/36 ; G06F15/16 ; H04L12/46 ; H04L12/28

TI - Data width variable type crossbar-switch apparatus - enables communication via specific port using another board of larger data width, when data widths of communicating boards are different

PR - JP19980103232 19980415

PN - JP3189783B2 B2 20010716 DW200142 G06F13/36 033pp
- JP11296473 A 19991029 DW200003 G06F13/36 034pp

PA - (NIDE) NEC CORP

IC - G06F13/36 ;G06F15/16 ;G06F15/173 ;G06F15/177 ;H04L12/28 ;H04L12/46

AB - JP11296473 NOVELTY - Several boards are connected to a set of ports with same data width. A cross bar switch (5) connects input ports (6-1-6-4), data ports (7-1-7-4) and address control ports (8-1-8- 4) between processor boards (2-1,2-2) and memory boards (3-1,3- 2). When the data widths of the communicating boards are different, the communication is performed via specific port using another board with larger data width. DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following: cross bar switch unit connecting method; control program recorded in recording medium
- USE - Data width variable type crossbar-switch apparatus.
- ADVANTAGE - Enables communication with narrow width as well as broad width ports. DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the data width variable type crossbar-switch apparatus. (2-1,2-2) Processor boards; (3-1,3-2) Memory boards; (5) Crossbar switch; (6-1-6-4) Input ports; (7-1-7-4) Data ports; (8-1-8-4) Address control ports.
- (Dwg.1/40)

OPD - 1998-04-15

AN - 2000-028977 [03]

PN - JP11296473 A 19991029

PD - 1999-10-29

AP - JP19980103232 19980415

IN - YOKOYAMA ATSUSHI

PA - NEC CORP

TI - DATA WIDTH VARIABLE TYPE CROSSBAR SWITCHING DEVICE, CONNECTION METHOD THEREFOR, AND MEDIUM FOR STORING CONTROL PROGRAM FOR THE DEVICE

AB - PROBLEM TO BE SOLVED: To provide a data width variable type crossbar switching device which can communicate regardless of the data width of another port even during communication between a port of a narrower data width and a port of a broader data width connected to the crossbar switch.

- SOLUTION: Communication with another port is executed using empty ports of the board of a wider data width when communicating through crossbar switch side input/output parts6-1 to 6-4, data parts 7-1 to 7-4 and address control parts 8-1 to 8-4 arranged between processor boards 2-1 and 2-2, memory boards 3-1 and 3-2, and a cross bus switch 5 wherein data widths are different among communicating boards. Data are sorted for each communicated party by the data parts7-1 to 7-4, the sorted data are retained in each of buffer group of two systems. The address control parts 8-1 to 8-4 instruct path of input/output data to the data parts 7-1 to 7-4.

I - G06F13/36 ;G06F13/36 ;G06F15/16 ;H04L12/46 ;H04L12/28

65531

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(54) Title: DATA WIDTH VARIABLE TYPE CROSSBAR SWITCH DEVICE, AND CONNECTION METHOD, AND RECORDED CONTROL PROGRAM FOR THE RECORD MEDIUM

(57) Abstract:
[Problem to be solved] To provide a data width variable type crossbar switching device, which can communicate regardless of the data, width of another port even during communication between a narrower port data width and a broader/wider port data width connected to the crossbar switch.
[Solution] Communication with another port is executed using empty ports of the board of a wider data width when communicating through crossbar switch side input/output parts 6-1 to 6-4, data parts 7-1 to 7-4 and address control parts 8-1 to 8-4 arranged between processor boards 2-1 and 2-2, memory boards 3-1 and 3-2, and a crossbar switch 5 wherein data widths are different among communicating boards. Data are sorted for each communicated party by the data parts 7-1 to 7-4, the sorted data are retained in each of buffer group of two systems. The address control parts 8-1 to 8-4 instruct path of input/output data to the data parts 7-1 to 7-4.

CLAIMS

[Claim 1] It has a plurality of ports of the same data width where a plurality of boards is connected. It is a data width variable type crossbar switch device, which connects between said plurality of boards through said plurality of ports. The data width variable type crossbar switch device is characterized by constitution so that the communication with other boards may be performed through the port which has empty ports where a board with said wide data width is connected, in case the data width of the boards with which communication differs.

[Claim 2] It has a plurality of ports of the same data width where a plurality of boards is connected. It is a data width variable type crossbar switch device, which connects between said plurality of boards through said plurality of ports. A detection means to detect the port which has empty ports where a board with said wide data width is connected in case the data width of the boards which communication differs, data width variable type crossbar switch device characterized by having a means to perform the communication with other boards through the port detected with said detection means.

[Claim 3] Data width variable type crossbar switch device according to claim 2 characterized by constitution so that said plurality of ports may be assigned to a board with said wide data width.

[Claim 4] Said detection means is a data width variable type crossbar switch device according to claim 3 characterized by constitution so that the port which is empty out of a plurality of ports assigned to the board with said wide data width may be detected.

[Claim 5] Said detection means is a data width variable type crossbar switch device according to claim 3 or 4 characterized by constitution so that said plurality of ports in use may be specially designated based on address information from the ports of each assigned to the board with said wide data width.

[Claim 6] Said detection means is a data width variable type crossbar switch device according to claim 3 to claim 5 characterized by including a memory means to memorize the information on the port assigned to a plurality of said boards of each, and a communication partner board on each of the port assigned to said plurality of board of each, and retention means to retain information which specifically designates the ports of each, which are assigned to proper board.

[Claim 7] Data width variable type crossbar switch device according to claim 2 to claim 6 characterized by including containing means to contain the data with which proper board is delivered and received between proper board and communication partners with said wide data width in the board.

[Claim 8] Data width variable type crossbar switch device according to claim 2 to claim 7 characterized by including a setting means to set up the I/O path of the data

delivered and received between proper boards with said wide data width and communication partners.

[Claim 9] It has plurality of ports of the same data width where plurality of boards is connected. It is the connection method of the data width variable type crossbar switch device, which connects between said plurality of boards through said plurality of ports. The connection method of the data width variable type crossbar switch device characterized by performing the communication with other boards through the port which has empty ports where a board with said wide data width is connected with the data width of the boards which communication differs.

[Claim 10] It has plurality of ports of the same data width where plurality of boards is connected. It is the connection method of the data width variable type crossbar switch device, which connects between said plurality of boards through said plurality of ports. The step which detects the port which has empty ports where a board with said wide data width is connected in case the data width variable type crossbar switch device characterized by having the step which performs the communication with other boards through the detected port.

[Claim 11] The connection method of the data width variable type crossbar switch device according to claim 10 characterized by assigning said plurality of ports to a board with said wide data width.

[Claim 12] The step which detects said empty port is the connection method of the data width variable type crossbar switch device according to claim 11 characterized by constitution so that the port which is empty out of plurality of ports assigned to the board with said wide data width may be detected.

[Claim 13] The step which detects said empty port is the connection method of the data width variable type crossbar switch device according to claim 11 or 12 characterized by specially designating a port in use of said plurality of ports based on a plurality of address information from the ports of each assigned to the board with said wide data width.

[Claim 14] The step which detects said empty port is the connection method of the data width variable type crossbar switch device according to claim 11 to claim 13 characterized by memory means to memorize information on the port assigned to said plurality of boards of each, so that said empty port may be detected using a retention means to retain the information which specially designates the ports of each which were assigned to the board and the board of a communication partner for every port.

[Claim 15] The connection method of the data width variable type crossbar switch device according to claim 11 to claim 14 characterized by containing the data delivered and received between proper boards and communication partners by one side of the 1st and 2nd containing means by which said data width has the data width of a board.

[Claim 16] The connection method of the data width variable type crossbar switch device according to claim 10 to claim 15 characterized by including the step which sets up the I/O path of the data delivered and received between boards and communications partners with said wide data width.

[Claim 17] It has a plurality of ports of the same data width where a plurality of boards is connected. It is the record medium which recorded the connection control program for making the processing which connects between said plurality of boards through said plurality of ports perform to a processor. Said connection control program is the record medium which recorded the connection control program characterized by making the communication with other boards perform to said processor through the port which has empty ports where a board with said wide data width is connected in case the data width of the boards differ in communication.

[Claim 18] It has a plurality of ports of the same data width where a plurality of boards is connected. It is the record medium which recorded the connection control program for making the processing which connects between said plurality of boards through said plurality of ports perform to a processor. Said connection control program makes the port which has empty ports where a board with said wide data width is connected to it in case the data width of the boards which communication differs in said processor detect. The record medium that recorded the connection control program characterized by making the communication with other boards performs through the detected port.

[Claim 19] Said connection control program is the record medium which recorded the connection control program according to claim 18 characterized by making the port which is empty out of a plurality of ports assigned to the board with said wide data width to detect in case said processor is made to detect said empty port.

[Claim 20] Said connection control program is the record medium which recorded the connection program according to claim 18 or 19 characterized by making a port in use of said plurality of ports specially designated based on a plurality of address information from the ports of each assigned to the board with said wide data width in case said processor is made to detect said empty port.

[Claim 21] A memory means to memorize the information on the port assigned to said plurality of boards of each, in case said connection control program makes said processor detect said empty port, on said plurality of boards of each claim 18 to claim 20 characterized by making said empty port detect using a retention means to retain the information which specially designates the assigned ports of each which were assigned to the board and the board of a communications partner for every port either the connection control program or the recorded record medium.

[Claim 22] Said connection control program, claim18 to claim 21 characterized by making the data delivered and received between boards and communication partners by one side of the 1st and 2nd containing means which the data width of a board with said

wide data width in said processor store is the record medium which recorded the connection control program.

[Claim 23] Said connection control program, claim 18 to claim 22 characterized by making the I/O path of the data delivered and received between boards and communication partners with said wide data width set it as said processor is the record medium which recorded the connection control program.

[Detailed Description of the Invention]
[0001]
[Technical Field of the Invention] This invention relates to the crossbar switch device which connects between ports with especially different data width about the record medium which recorded the control program on data width variable type crossbar switch device and its connection method line up.

[002]
[Description of the prior art] In this kind of crossbar switch device, as shown in Fig. 39, the processor board (#1-#3) 2-1 to 2-3, the memory board (#1-#3) 3-1 to 3-3, and the I/O (I/O) board (#1-#6) 4-1 to 4-6 are mutually connected through a crossbar switch 5.

[0003] In this case, it has data width each different, respectively in the processor board (#1-#3) 2-1 to 2-3, the memory board (#1-#3) 3-1 to 3-3, and the I/O (I/O) board (#1-#6) 4-1 to 4-6. That is, the crossbar switch 5 has connected between the ports of different data width.

[0004] Here as shown in the processor board (#1) 2-1 at Fig. 40, the processor 21-1, the controller 22-1, the input buffer 23-1, and the output buffer 24-1 are carried, and they are mutually connected by bus 200-1 in a board.

[0005] In addition, although not illustrated, it has the same constitution as other processor boards (#2, #3) 2-2 and the processor board (#1) 2-1 of the above. Moreover, although not illustrated like the above, the memory board (#1-#3) 3-1 to 3-3 and the I/O (I/O) board (#1-#6) 4-1 to 4-6 also have the same constitution as the above-mentioned processor board (#1) 2-1 except carrying memory and I/O instead of a processor 21-1.

[0006] The above crossbar switch device is performing the communication in the ports of the same data width because a controller 22-1 controls an input buffer 23-1 and an output buffer 24-1.

[0007]
[Problems to be solved by the Invention] Although between the ports of the data width from which the crossbar switch differs is connected with the prior crossbar switch device mentioned above, if between different data width is connected with a crossbar switch, and it is communicating between ports where data width is narrow, the transfer between the ports where data width is wide cannot be performed.

[0008] Moreover, about a high part possibility of a concurrent access demand of the parts of memory etc. can solve the above-mentioned problem by preparing another wide transfer path of data width, in that case, a utilization efficiency will become low and will cause an increase in the amount of hardware.

[0009] Furthermore, although the above-mentioned technical problem is also solvable in terms of keeping wait where a plurality of data width port is narrow on a plurality of the same board instead of being the port where data width is wide, plurality of the address lines and the controllers which connect a relevant board and a crossbar switch will also be needed, and will cause large increase in the amount of hardware.

[0010] Then, it is the purpose of this invention to solve the above-identified problem, and provide the data width variable type crossbar switch device, which can communicate without regarding the data width of the opponents port in communication with narrow data port, in the wide data width port connected to the crossbar switch, the connection method, and the record medium which record the control program.

[0011]
[Means for solving the problem] The data width variable type crossbar switch device by this invention has a plurality of ports of the same data width where each plurality of boards is connected. It is the data width variable type crossbar switch device, which connects between said plurality of boards through said plurality of ports. In case the data width of the boards that communicate differs, it constitutes so that the communication link with other boards may be performed through the port, which has empty ports where a board with wide data width is connected.

[0012] Other data width variable type crossbar switch device by this invention has a plurality of ports of the same data width where each plurality of boards is connected. It is the data width variable type crossbar switch device, which connects between said plurality of boards through said plurality of ports. It has a detection means to detect the port which has empty ports where a board with wide data width is connected in case the data width of the boards which communicate differs, and a means to perform the communication with other boards through the port detected with said detection means.

[0013] The connection method of the data width variable type crossbar switch device by this invention has a plurality of ports of the same data width where each plurality of boards is connected. It is the connection method of the data width variable type crossbar switch device, which connects between said plurality boards through said plurality ports. In case the data width of the boards that communicate differs, it is made to perform the communication with other boards through the port, which has empty ports where a board with wide data width is connected.

[0014] The connection method of other width variable type crossbar switch device by this invention has a plurality of ports of the same data width where each plurality of boards is connected. It is the connection method of the data width variable type crossbar switch device that connects between said plurality of boards through said plurality of

ports. It has the step that detects the port that has empty ports where a board with wide data width is connected in case the data width of the boards that communicate differs, and the step that performs the communication with other boards through the detected port.

[0015] The record medium which recorded the connection control program by this invention has a plurality of ports of the same data width where each plurality of boards are connected. It is the record medium which recorded the connection control program for making the processor which connects between said plurality of boards through said plurality of ports perform to a processor. Said connection control program is making the communication with other boards perform to it through the port which has empty ports where a board with wide data width is connected, in case the data width of the boards which communication differs in said processor.

[0016] The record medium which recorded other connection control programs by this invention has a plurality of ports of the same data width where each plurality of boards are connected. It is the record medium which recorded the connection control program for making the processing which connects between said plurality of boards through said plurality of ports perform to a processor. In case the data width of the boards which communicate differs in said processor, said connection control program makes it detect the port which has empty ports where a board with wide data width is connected, and is making the communication with other boards perform to it through the detected port.

[0017] That is, the data width variable type crossbar switch device of this invention can be made to communicate with other boards in the empty port for which the side held by the board in which the data width has a wide port, in case the data width of the same board which communication differs.

[0018] Namely, the switch in a board is formed and data are distributed for every communications partner. Moreover, in addition to the switch in a board, two buffer groups in which data width has the same data width as the maximum data width of a wide port are prepared in data division, and the data which were able to be distributed with the switch in a board are saved. The switch control section in a board is instructed on each switch (SW) in which the path of an I/O data was prepared by the switch in a board based on the signal from the address control section in a board.

[0019] As mentioned above, data width becomes possible to carry out division use of the port to the crossbar switch in a board with a wide port by having the setup system which stores two data, and the controlling mechanism which distributes data.

[0020]
[Embodiment of the Invention] Next, one example of this invention is explained with reference to a figure. Fig. 1 is the block diagram showing the configuration of the crossbar switch device by one example of this invention. In the figure, crossbar switch device 1 is equipped with a crossbar switch 5 and the crossbar switch side I/O section 6-1 to 6-4, and data division 7-1 to 7-4 and the address control section 8-1 to 8-4 are arranged

corresponding to the processor board 2-1 with wide data width (#1, #2), 2-2 and the memory board (#1, #2) 3-1, and 3-2 each.
[0021] The crossbar switch 5 had 12 128-bit ports, connected to the 128-bit port the I/O (I/O) board (#1-#4) 4-1 to 4-4 whose data width is 128-bit width as it was, and is connected to two 128-bit ports the processor board 2-1 whose data width is 256-bit width, 2-2 and the memory board 3-1, and 3-2.

[0022] That is, crossbar switch device 1 is connected through the crossbar switch side I/O section 6-1 to 6-4 by which the processor board 2-1, 2-2 and the memory board 3-1, and 3-2 were connected to two ports of a crossbar switch 5.

[0023] By the crossbar switch side I/O section 6-1 to 6-4, above-mentioned data division 7-1 to 7-4, and the above-mentioned address control section 8-1 to 8-4 in case the data width of the boards which communicate differs (for example, the processor board 2-1, 2-2 and the memory board 3-1, and 3-2 have data width larger then the I/O board (#1-#4) 4-1 to 4-4) It can be made to perform the communication with other boards in the empty port as for which the side held by the board in which the data width has a wide port.

[0024] That is, the switch in a board (not shown) is formed in data division 7-1 to 7-4, and data are distributed for every communication partner. Moreover, in addition to the switch in a board, two buffer groups (not shown) of 256-bit width are prepared in data division 7-1 to 7-4, and the data which were able to be distributed with the switch in a board are saved by two buffer groups in each.

[0025] The switch control section in a board (not shown) prepared in the address control section 8-1 to 8-4 is directed on each switch (SW) in which the path of a I/O data was prepared by the switch in a board based on the signal from the address control section in a board (not shown).

[0026] As mentioned above, data width becomes possible to carry out division use of the port to the crossbar switch 5 in a board with a wide port by having the setup system which stores two data, and the controlling mechanism which distributes data.

[0027] In addition, in the one example of this invention, crossbar switch device 1 was used as the address/data discrete type, with the signal decided beforehand, using the address line, reservation of a communication path, transfer initiation, transfer termination, etc. were performed, and the structure which can output and input suitable data is realized.

[0028] Figure 2 is the block diagram showing the configuration of the crossbar switch side I/O section 6-1 of fig. 1. In the figure, the crossbar switch side I/O section 6-1 is equipped with the crossbar switch side address control section 61-1.

[0029] It connects with two ports of a crossbar switch 5 with the address line (A) and the 128-bit data line (D), and the crossbar switch side I/O section 6-1 is connected to the

processor board 2-1 with the address line (A), a identification bit (bit) (Sa, Sb), and the two 128-bit data lines (a, b).

[0030] The crossbar switch side address control section 61-1 inputs the address from two ports, and outputs the address and a identification bit to the processor board 2-1. In addition, although not illustrated, other crossbar switch side I/O sections 6-2 to 6-4 have the same composition as the above-mentioned crossbar switch side I/O section 6-1.

[0031] Fig. 3 is the block diagram showing the configuration of the data division 7-1 of Fig. 1. In the figure, data division 7-1 consist of the switch 71-1 in a board, a buffer 72-1 and 73-1, a switch (SW#1-SW#3) 74-1, 75-1 and 76-1, a buffer A 77-1, and a buffer group B 78-1. In addition, other data divisions 7-2 to 7-4 have the same composition as the above-mentioned data division 7-1.

[0032] Fig. 4 is the block diagram showing the configuration of the address control section 8-1 of Fig. 1. In the figure, the address control section 8-1 is equipped with the address control section 81-1 in a board, and the switch control section 82-1 in a board. In addition, other address control section 8-2 to 8-4 have the same composition as the above-mentioned address control section 8-1.

[0033] Fig. 5 is the block diagram showing the configuration of the switch 71-1 in a board of Fig. 3. In the figure, the switch 71-1 in a board is equipped with switch (SW#11-SW#20) 71a-1 to 71j-1.

[0034] Fig. 6 is a drawing showing the example of a configuration of a switch. Fig. 6(a) shows the configuration of switch (SW#11-SW#16) 71a-1 to 71f-1 shown in the switch (SW#2, SW#3) 75-1 shown in Fig. 3, 76-1, and Fig. 5. Fig. 6(b) shows the configuration of switch (SW#17-SW#20) 71g-1 to 71j-1 shown in the switch (SW#1) 74-1 shown in Fig. 3 and Fig. 5.

[0035] Fig. 7 is the block diagram showing the configuration of the crossbar switch side address control section 61-1 shown in Fig. 2. The crossbar switch side address control section 61-1 consists of controller 61a-1, Memory (A) 61b-1, and Memory (B) 61c-1.

[0036] Fig. 8(a) is a drawing showing the contents of memory of Memory (A) 61b-1 of Fig. 7, and Fig. 8(b) is a drawing showing the contents of memory of Memory (B) 61c-1 of Fig. 7. In these drawings, the board name (processor #1, processor #2, memory #1, memory #2, I/O#1, I/O#2, I/O#3, I/O#4) and the port name (a,b) are matched and memorized to Memory (A) 61b-1.

[0037] Moreover, to Memory (B) 61c-1, the communication partner point board name of b port and the communication partner point port name of b port were matched, and the communication partner point board name a port and the communication partner point port name of a port are memorized again.

[0038] Fig. 9 is a block diagram showing the configuration of the address control section 81-1 in a board of fig. 4. In the figure, the address control section 81-1 in a board consists of controller 81a-1, Memory (C) 81b-1, Memory (D) 81c-1, and counter 81d-1 to 81g-1.

[0039] Fig. 10(a) is a figure showing the contents of the memory of Memory (C) 81b-1 of Fig. 9, and Fig. 10(b) is a figure showing the contents of the memory of Memory (D) 81c-1 of Fig. 9. In these drawings, the value of the current discernment bit Sa and the value of the current discernment bit Sb, and the value of the discernment bit Sa in front of 1 clock and the value of the discernment bit Sb in front of clock are memorized by Memory (C) 81b-1.

[0040] Moreover, the address information for buffer A group 77-1 and the order information of data forwarding, and the address information and the order information of data forwarding for buffer B group 78-1 and memorized by Memory (D) 81c-1.

[0041] Here, address information AA1, AA2, AA3, and AA4 and ...show the contents of an address line signal sent in relation to the data included in the buffer A group 77-1, and the order information NAA1, NAA2, NAA3, and NAA4 of data forwarding and ...show that the corresponding address line signal content and the simultaneously sent from which data were sent from which data block head.

[0042] Address information AB1, AB2, AB3, and AB4 and ...show the contents of an address line signal sent in relating to the data included in the buffer B group 78-1, and the order information NAB1, NAB2, NAB3, and NAB4 of data forwarding, and ... show that the corresponding address line signal content and the simultaneously sent data were sent from which data block head.

[0043] Fig. 11 is a figure showing the switch (SW#1-SW#3) 74-1 to 76-1 of Fig. 3 by the switch control section 82-1 in a board of Fig. 4, and control of Fig. 5 of switch (SW#11-SW#20) 71a-1 to 71j-1.

[0044] When connecting with Port c from the port a of the switch 71-1 in a board shown in Fig. 3 and Fig. 5 (a →c), and when connecting with port d from port b (b→d), the switch control section 82-1 in a board it controls so that switch (SW#11) 71a-1, switch (SW#13) 71c-1, switch (SW#16) 71f-1, and switch (SW#17) 71g-1 are connected to the "1" side.

[0045] At this time, a switch (SW#1-SW#3) 74-1 to 76-1, switch (SW#14) 71d-1, switch (SW#15) 71e-1, switch (SW#19) 71i-1, and switch (SW#20) 71j-1 may be connected to any by the side of "1" a side and "0". In Fig. 11, "-" shows this condition.

[0046] When connecting with port e from the port a of the switch 71-1 in a board (a→e), and when connecting with port f from port b (b→f), the switch control section 82-1 in a board it controls so that a switch (SW#2) 75-1, a switch (SW#3) 76-1, switch (SW#11) 71a-1, and switch (SW#20) 71j-1 are connected to the "0" side, and switch (SW#12) 71b-

1, switch (SW#13) 71c-1, switch (SW#16) 71f-1, and switch (SW#19) 71i-1 are connected to the "1" side.

[0047] At this time, a switch (SW#1) 74-1, switch (SW#14) 71d-1, switch (SW#15) 71e-1, switch (SW#17) 71g-1, and switch (SW#18) 71h-1 may be connected to any by the side of "1" and "0" side.

[0048] When connecting with ports c and d from the port a of the switch 71-1 in a board (a→c, d), the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "0" sides. The switch control section 82-1 in a board by synchronizing with the clock of a crossbar switch 5, controls Switch (SW#11) 71a-1 moreover, to the "1" side and "0" side, switch (SW#13) 71c-1 to ("1" or "0") and "0" side, switch (SW#14) 71d-1 to "0" sides and ("1" or "0") and "1" side, switch (SW#17) 71g-1 ("1" or "0") and "1" side, switch (SW#18) 71h-1 "1" and ("1" or "0") so that each one is repeatedly, and alternately connected.

[0049] At this time, a switch (SW#1) 74-1, switch (SW#12) 71b-1, switch (SW#15) 71e-1, switch (SW#16) 71f-1, switch (SW#19) 71i-1, and switch (SW#20) 71j-1 may be connected to any by the side of "1" and "0" side.

[0050] When connecting with ports e and f from the port a of the switch 71-1 in a board (a→e, f), the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "0" sides. The switch control section 82-1 in a board by synchronizing with the clock of a crossbar switch 5, controls switch (SW#11) 71a-1 moreover, to the "1" side and "0" side, switch (SW#13) 71c-1 ("1" or "0") and "0" side, switch (SW#14) 71d-1 to "1" sides and ("1" or "0") and "1" side, switch (SW#19) 71i-1 ("1" or "0") and "1" side, switch (SW#20) 71j-1 "1" and ("1" or "0") so that each one is repeatedly, and alternately connected.

[0051] At this time, a switch (SW#1) 74-1, switch (SW#12) 71b-1, and switch (SW#15-SW#18) 71e-1 to 71h-1 may be connected to any by the side of "1" and "0" side.

[0052] When connecting with ports c and d from the port b of switch 71-1 in a board (b→c, d), the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "0" sides. The switch control section 82-1 in a board by synchronizing with the clock of a crossbar switch 5, controls switch (SW#12) 71b-1 moreover, to the "1" side and "0" side, switch (SW#15, SW#17) 71e-1 and 71g-1 to ("1" or "0") and "0" side, switch (SW#16, SW#18) 71f-1 and 71h-1 "0" and ("1" or "0") so that each one is repeatedly and alternately connected.

[0053] At this time, a switch (SW#1) 74-1, switch (SW#11) 71a-1, switch (SW#13) 71c-1, switch (SW#14) 71d-1, switch (SW#19) 71i-1, and switch (SW#20) 71j-1 may be connected to any by the side of "1" and "0" side.

[0054] When connecting with ports e and f from the port b of the switch 71-1 in a board (b→e, f), the switch control section 82-1 in a board is controlled so that a switch (SW#2)

75-1 and a switch (SW#3) 76-1 are connected to the "0" sides. The switch control section 82-1 in a board by synchronizing with the clock of a crossbar switch 5, switch (SW#12) 71b-1 moreover, to the "1" side and "0" side, switch (SW#15) 71e-1 to ("1" or "0") and "1" side, switch (SW#16) 71f-1 to ("1" or "0") and "0" side, switch (SW#19) 71i-1 ("1" or "0") and "0" side, switch (SW#20) 71j-1 "0" side and ("1" or "0") so that each one is repeatedly and alternately connected.

[0055] At this time, a switch (SW#1) 74-1, switch (SW#11) 71a-1, switch (SW#13) 71c-1, switch (SW#14) 71d-1, switch (SW#17) 71g-1, and switch (SW#18) 71h-1 may be connected to any by the side of "1" and "0"side.

[0056] When connecting with port a from the ports c and d of the switch 71-1 in a board (c, d→a), the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "1" side. The switch control section 82-1 in a board by synchronizing with the clock of a crossbar switch 5, controls switch (SW#11) 71a-1 moreover, to the "0" side and "1" side, switch (SW#13) 71c-1 to ("1" or "0") and "0" side, switch (SW#14) 71d-1 to ("1" or "0") and "0" side, switch (SW#17) 71g-1 "1"side and "("1" or "0"), switch (SW#18) 71h-1 "1" and ("1" or "0") so that each one is repeatedly and alternately connected.

[0057] At this time, a switch (SW#1) 74-1, switch (SW#12) 71b-1, switch (SW#15) 71e-1, switch (SW#16) 71f-1, switch (SW#19) 71i-1, and switch (SW#20) 71j-1 may be connected to any by the side of "1" and "0" side.

[0058] When connecting with port b from the ports c and d of the switch 71-1 in a board (c, d→b), the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "1" side. The switch control section 82-1 in a board by synchronizing with the clock of a crossbar switch 5, controls switch (SW#12) 71b-1 moreover, to the "0" side and "1" side, switch (SW#15) 71e-1 to ("1" or "0") and "0" side, switch (SW#16) 71f-1 to ("1" or "0") and "0" side, switch (SW#19) 71i-1 "0" side and ("1" or "0"), switch (SW#20) 71j-1 ("1"or "0") and "1" so that each one is repeatedly and alternately connected.

[0059] At this time, a switch (SW#1) 74-1, switch (SW#11) 71a-1, switch (SW#13) 71c-1, switch (SW#14) 71d-1, switch (SW#17) 71g-1, and switch (SW#18) 71h-1 may be connected to any by the side of "1" and "0" side.

[0060] When connecting with the output side of the switch 71-1 in a board, the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "0" sides.

[0061] At this time, a switch (SW#1) 74-1 and switch (SW#11-SW#20) 71a-1 to 71j-1 may be connected to any by the side of "1" and "0" side.

[0062] When connecting with the input side of the switch 71-1 in a board, the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "1" side.

[0063] At this time, a switch (SW#1) 74-1 and switch (SW#11-SW#20) 71a-1 to 71j-1 may be connected to any by the side of "1" and "0" side.

[0064] When the switch 71-1 in a board is connected to the output of the buffer A group 77-1, the switch control section 82-1 in a board is controlled so that a switch (SW#1) 74-1 is connected to the "1" side.

[0065] At this time, a switch (SW#2, SW#3) 75-1, 76-1, and switch (SW#11-SW#20) 71a-1 to 71j-1 may be connected to any by the side of "1" and "0" side.

[0066] When the switch 71-1 in a board is connected to the output of the buffer B group 78-1, the switch control section 82-1 in a board is controlled so that a switch (SW#1) 74-1 is connected to the "0" sides.

[0067] At this time, a switch (SW#2, SW#3) 75-1, 76-1, and switch (SW#11-SW#20) 71a-1 to 71j-1 may be connected to any by the side of "1" and "0" side.

[0068] With reference to the fig. 1 to fig. 11, the crossbar switch device 1 by one example of this invention is explained. It connects with each port of a crossbar switch 5, and the I/O board (#1-#4) 4-1 to 4-4 is using only a part for one port of a crossbar switch 5.

[0069] On the other hand, it connects with each port of a crossbar switch 5 through the crossbar switch side I/O section 6-1 to 6-4 shown in fig. 2, and the processor board 2-1, 2-2 and the memory board 3-1, and 3-2 are using a part for two ports of a crossbar switch 5.

[0070] The crossbar switch side I/O section 6-1 to 6-4 is connected to the data division 7-1 to 7-4 and the address control section 8-1 to 8-4 in each board shown in fig. 3 and fig. 4. The crossbar switch side I/O section 6-1 to 6-4, after confirming empty board (by a discernment bit) to the transfer request via the conventional crossbar switch, answer the (yes or no), and also request the transfer to the crossbar switch side address control section 61-1 to which the suitable board was connected in a response to the transfer request from the connected board.

[0071] The data division 7-1 to 7-4 in each board shown in fig. 3 consist of the switch 74-1 for data distribution, 75-1, 76-1, two buffer A groups 77-1, and a buffer B group 78-1. The address control section 8-1 to 8-4 in each board shown in fig. 4 consists of an address control section 81-1 in a board, and a switch control section 82-1 in a board.

[0072] From the plurality of interconnection of switch 71a-1 to 71j-1 shows the switch 71-1 in a board of data division 7-1 to 7-4 in fig. 5, the directions from the switch control

section 82-1 in a board being based on each switch 71a-1 to 71j-1 is changed. Without gathering the input data to each board for every port, and the conventional board being conscious of data width, the buffer A group 77-1 and the buffer B group 78-1 hold data by 256-bit width so that data can be received.

[0073] The address control section 81-1 in a board of the address control section 8-1 to 8-4, as shown in fig. 9, the address line of the crossbar switch 5, and the discernment bit line (Sa, Sb), and the a, b port discernment line, and the prior signal line to the controller 22-1 device shown in fig. 40, the signal line for data incorporation timing to the buffer A group 77-1 and the buffer B group 78-1 connects with the 128-bit buffer 72-1 of the preceding paragraph, and the signal line for data incorporation timing of 73-1 at the signal line for data incorporation timing to the input buffer 23-1 conventional device.

[0074] The address control section 81-1 in a board updates a discernment bit response to the transfer request from the prior controller 22-1 device, and performs a transfer request to a crossbar switch 5 side. Moreover, the address control section 81-1 in a board recognizes the width and the port of a data which are transmitted from the information on a discernment bit in response to the transfer request from a crossbar switch 5 side, incorporates data to the buffer A group 77-1 and the buffer B group 78-1, and transmits the data to the timing of the opening of the data I/O section device.

[0075] The switch control section 82-1 in a board will direct by changing to a required switch with reference to the contents shown in fig. 11, if the directions from the address control section 81-1 in a board are received.

[0076] If fig. 7 is referred to, the configuration of the address control section 61-1 in the crossbar switch side I/O section 6-1 shown in fig. 2 is shown, and the address control section 61-1 consists of controller 61a-1, Memory (A) 61b-1, Memory (B) 61c-1.

[0077] Memory (A) 61b-1 becomes a means for getting to know whether the whole configuration environment of the crossbar switch device 1 is memorized, and [referring to fig. 8(a)] and the corresponding communications partner have the possibility of a 256 bit width transfer. In case Memory (B) 61c-1 memorizes a partner's board name and port name under current communication and it transmits the signal [refer to fig. 8(b)] and the address line it is referred to.

[0078] If fig. 9 is referred to, the detailed configuration of the address control section 81-1 in a board shown in fig. 4 is shown, and the address control section 81-1 in a board consists of controller 81a-1, Memory (C) 81b-1, Memory (D) 81c-1, and the counter 81d-1 to 81g-1.

[0079] Memory (C) 81b-1 becomes a means for controller 81a-1 to get to know that from which the value in front of 1 clock of the discernment bits Sa and Sb was held, and the value changed with [refer to fig. 10(a)] an applicable clock.

[0080] Memory (D) 81c-1 the contents AA1, AA2, AA3, and AA4 of an address signal sent with the data of the buffer A group 77-1 of data division 7-1, and the buffer B group 78-1, ...AB1, AB2, AB3 and AB4, and simultaneously sending data, specifying record NAA1, NAA2, NAA3, NAA4,... NAB1, NAB2, NAB3, NAB4... held together [reference fig.10(b)].

[0081] Counter 81d-1 to 81g-1 shows the offer of the data of the position?? of a block in the prior data input section device with whether it enters to the buffer A group 77-1 and the buffer B group 78-1.

[0082] When sending the clock for data incorporation to the buffer A group 77-1 and the buffer B group 78-1, this count-up instructions are outputted to applicable counter 81d-1 simultaneously. When sending data incorporation instruction to the buffer of the data input section of conventional device, output count-down instructions to counter 81d-1 and 81f-1, and count-up instructions are outputted to simultaneously counter 81e-1 and 81g-1. It realizes by sending zero reset instructions to counter 81e-1 and 81g-1 with data incorporation instructions of the last of the block data to the buffer of the data input section of conventional device.

[0083] Fig. 12 to fig.15 are flow charts which show the actuation of the crossbar switch side address control section 61-1 shown in fig.2 and fig. 7, and fig.16 to fig. 23 are flow charts which show the actuation of the address control section 81-1 in a board shown in fig. 4 and fig. 9.

[0084] With reference to the fig. 1 to fig. 23, actuation of the crossbar switch device by one example of this invention is explained. In addition, performing the program of the control memory, which each control section does not illustrate, can also be realized, and actuation of the above-mentioned flow chart has usable ROM (read-only memory) etc, as a control memory.

[0085] Fig. 12 to fig.15 show actuation in case the processor board 2-1 by which direct continuation was carried out to the crossbar switch side address control section 61-1 performs a transfer request. In this case, the crossbar switch side address control section 61-1 will check the empty situation of the port of a self-circuit with reference to a discernment bit, if the processor board 2-1 connected is a 256-bit board when a transfer request is received through the address line from the address control section 81-1in a board of the address control section 8-1 of the processor board 2-1 (fig. 12 step S1) (fig. 12 step S2) (fig. 12 step S3).

[0086] If 256 bit of port of crossbar switch 5 are securable (fig. 12 step S4) if two ports of the crossbar switch 5 to which the crossbar switch side I/O section 6-1 is connected are securable, the crossbar switch side address control section 61-1 will check the maximum data with of a communications partner with reference to Memory (A) 61b-1 (fig. 12 step S5).

[0087] The crossbar switch side address control section 61-1 will send a transfer request to the two address lines corresponding to the ports a and b of a communications partner, if the maximum data width of the communications partner is 256-bit width (fig. 12 step S6) (fig. 12 step S7), and if it is 128 bits, it will send a transfer request to one address line corresponding to the port of a communications partner (fig. 12 step S9).
[0088] The crossbar switch side address control section 61-1 will relay the signal to the address control section 81-1 in a board of the processor board 2-1, if transfer OK comes from both two address lines (fig. 12 step S8). The crossbar switch side address control section 61-1 relays a signal in the same path till transfer termination. (fig. 12 step S9).

[0089] On the other hand, the crossbar switch side address control section 61-1 changes the discernment bit corresponding to one of the ports into "0" by the approach decided beforehand (fig. 14 step S19), when there is transfer OK only from the one address line (fig. 14 step S18).

[0090] A discernment bit secures the near path of "1" and the crossbar switch side address control section 61-1 relays a transfer OK signal to the address control section 81-1 in a board of the processor board 2-1 (fig. 14 step S20).

[0091] In this case, the crossbar switch side address control section 61-1 records the path and partner's information which were secured to Memory (B) 61c-1 (fig. 14 step S20). Henceforth, it refers to, and checks the path and partner's information about the signal from the address control section 81-1 in a board, if it is a signal from the same communication partner, the junction of the signal will be continued till transfer termination (fig. 14 step S21). In addition, if the crossbar switch side address control section 61-1 becomes transfer termination, it will simultaneously eliminate the path information on Memory (B) 61c-1 (fig. 14 step S22).

[0092] The crossbar switch side address control section 61-1 relays the signal to the address control section 81-1 in a board of the processor board 2-1 (fig. 14 step S24), when a transfer failure comes on the contrary from both address lines (fig. 14 step S23).

[0093] On the other hand, if the port of the processor board 2-1 can secure only 128-bit width (fig. 12 step S10), the crossbar switch side address control section 61-1 is chosen by the approach which was able to determine the one address line of a partner beforehand, and sends a transfer request (fig. 12 step S11).

[0094] If transfer OK comes on the contrary to the transfer request (fig. 14 step S18), the crossbar switch side address control section 61-1 will secure a path like the above (fig. 14 step S20), and will relay transfer OK to the address control section 81-1 in a board of the processor board 2-1 (fig. 14 step S21).

[0095] Also in this case, the crossbar switch side address control section 61-1 records the path and partners information which were secured to Memory (B) 61c-1 (fig. 14 step S20). Henceforth, , it refers to, and checks the path and partner's information about the signal from the address control section 81-1 in a board, and if it is a signal from the same

communications partner, the junction of the signal will be continued till transfer termination (fig. 14 step S21). In addition, if the crossbar switch side address control section 61-1 becomes transfer termination, it will simultaneously eliminate the path information on Memory (B) 61c-1 (fig. 14 step S22).

[0096] The crossbar switch side address control section 61-1 relays the signal to the same address control section 81-1 in a board (fig. 14 step 23), also when a transfer failure comes on the contrary (fig. 14 step S24).

[0097] When the port of the processor board 2-1 is not 256-bits (fig. 12 step S2), the crossbar switch side address control section 61-1 relays the signal of a transfer request to the address line according to the data width of a communication partner with reference to Memory (A) 61b-1 (fig. 13 step S13).

[0098] The crossbar switch side address control section 61-1 will relay transfer OK to the address control section 81-1 in a board of the processor board 2-1 like the above, if transfer OK comes on the contrary to the transfer request (fig. 13 step S14). Henceforth, the crossbar switch side address control section 61-1 continues the junction of the signal till transfer termination (fig. 13 step S15).

[0099] The crossbar switch side address control section 61-1 relays the signal to the same address control section 81-1 in a board, also when a transfer failure comes on the contrary (fig. 13 step S16) (fig. 13 step S17).

[0100] Fig. 15 shows actuation when the crossbar switch side address control section 61-1 receives a transfer request from a crossbar switch 5 side. In this case, the crossbar switch side address control section 61-1 will check the empty situation of the port of a self-circuit with reference to a discernment bit, if a transfer request is received from a crossbar switch 5 side (fig. 15 step S31) (fig. 15 step S32).

[0101] If the processor board 2-1 to which the crossbar switch side address control section 61-1 is connected is a 256-bit board (fig. 15 step S33), a transfer request will judge whether it came from the two address lines (fig. 15 step S34).

[0102] It investigates whether the crossbar switch side address control section 61-1 can secure the port of a transfer request, if the transfer request is coming from the two address lines (fig. 15 step S35). If reservation of the port of a transfer request is possible, the crossbar switch side address control section 61-1, secures them by changing the discernment bits Sa and Sb into "1" (fig. 15 step S36), and transfer OK will be returned through the address line corresponding to the secured discernment bit (fig. 15 step S37).

[0103] The crossbar switch side address control section 61-1 transmits a transfer request to the address control section 81-1 in a board (fig. 15 step S38), a transfer path and partner information are memorized to Memory (B) 61c-1, and henceforth, with reference to the contents of Memory (B) 61c-1, if the signal from the applicable address line signal

from an applicable port, it will relay this to the address control section 81-1 in a board (fig. 15 step S39).

[0104] At this time, the address control section 81-1 in a board is an address signal from the data transfer point of a port, when 1-bit a and b port discernment line are "0", and it identifies that it is an address signal from the data transfer point of b port at the time of "1".

[0105] The crossbar switch side address control section 61-1 clears the contents of Memory (B) 61c-1 after transfer termination, and the discernment bit changed into "1" is returned (fig. 15 step S40).

[0106] If the processor board 2-1 connected is empty (fig. 15 step S33) and a corresponding port on the 128-bit board (fig. 15 step S41), the crossbar switch side address control section 61-1 will relay a transfer request as it is, and will relay and return the answerback to the empty situation of conventional device (fig. 15 step S42). Henceforth, the crossbar switch side address control section 61-1 performs the same actuation as the above (fig. 15 steps S38-S40).

[0107] If the corresponding port is not empty (fig. 15 step S14), if the port is not empty while the transfer request is not coming from the two address lines (fig. 15 steps S34 and S43), or if the crossbar switch side address control section 61-1 cannot secure the port of a transfer request (fig. 15 step S44), it returns a transfer failure in a path with a transfer request (fig. 15 step S47).

[0108] One crossbar switch side address control section 61-1 will change the discernment bit corresponding to an empty port into "1", if the port of a transfer request can be secured when a transfer request does not come from the two address lines (fig. 15 step S43), or if the port of a transfer request can secure while the transfer request is coming from the two address lines (fig. 15 step S44) (fig. 15 step S45).

[0109] The crossbar switch side address control section 61-1 returns transfer OK using the address line corresponding to the secured port (fig. 15 step S46), and performs the same actuation as the above henceforth (fig. 15 step S38-S40).

[0110] Actuation of the address control section 81-1 (not mounted in the 128-bit board) in a board of the address controller section 8-1 of the processor board 2-1 is shown in fig. 16- fig. 23. In this case, if a transfer request is received from the controller 22-1 (refer to fig. 40) of device by which direct continuation was carried out (fig. 16 step S51), the address control section 81-1 in a board will check that the ports c and d of the switch 71-1 in a board of the data division 7-1 of the processor board 2-1 are not used, and will relay a transfer request as it is (fig. 16 step S52). When used, a transfer failure is returned to a controller 22-1.

[0111] Then, the address control section 81-1 in a board receives the notice of transfer OK from the destination, and checks a discernment bit (fig. 17 steps S61 and S62) and a

256-bit band can be secured, namely it is Sa=1 and Sb=1 (fig. 17 step S63), direct a path to switch control section 82-1 in a board so that data can be directly sent out to this (fig. 17 step S64), namely the securing of the path c→a, and d→b, and modification of the sending side path of (SW#2, #3) 75-1.

[0112] Then, the address control section 81-1 in a board transmits the clock of a crossbar switch 5 to the output buffer 24-1 (refer to fig. 40) of conventional device, and enables sending out every clock and new data on a crossbar switch 5 (fig. 17 step S65).

[0113] The address control section 81-1 in a board relays the address-line signal from a controller 22-1 as it is till the completion of a transfer (fig. 17 step S66), and returns the discernment bits Sa and Sb to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (fig. 17 step S67).

[0114] The address control section 81-1 in a board will direct to operate in the mode which changes a path to the switch control section 82-1 in a board for every clock so that data can be sent in an order from c and d, if only 128 bit of bands are securable (fig. 17 step S68) (if discernment bits are Sa=1 and Sb=0), or if discernment bits are Sa=0 and Sb=1 (fig. 18 step S74).

[0115] When discernment bits are Sa=1 and Sb=0, the address control section 81-1 in a board directs reservation of a c→a path, and modification to a switch (SW#2, #3) 75-1 and the sending area of 76-1 to the switch control section 82-1 in a board (fig. 17 step S69).

[0116] Henceforth, it is directed to the switch control section 82-1 in a board that the address control section 81-1 in a board changes the path of c→a, and the path of d→a for every clock of a crossbar switch 5 (fig. 17 step S70). The address control section 81-1 in a board transmits the clock of a crossbar switch 5 to the output buffer 24-1 of conventional device once at 2 times, and enables sending out of data new once on a crossbar switch 5 at two clocks (fig. 17 step S71).

[0117] The address control section 81-1 in a board relays the address-line signal from a controller 22-1 as it is till the completion of a transfer (fig. 17 step S72), and returns the discernment bit Sa to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (fig. 17 step S73).

[0118] When discernment bits are Sa=0 and Sb=1, the address control section 81-1 in a board directs reservation of c→b path, and modification to a switch (SW#2, #3) 75-1 and the sending area of 76-1 to the switch control section 82-1 in a board (fig. 18 step S75).

[0119] Henceforth, it is directed to the switch control section 82-1 in a board that the address control section 81-1 in a board changes the path of c→b, and the path of d→b for every clock of a crossbar switch 5 (fig. 18 step S76). The address control section 81-1 in a board transmits the clock of a crossbar switch 5 to the output buffer 24-1 of

conventional device 2 times, and enables sending out new data once on a crossbar switch 5 at two clocks (fig. 18 step S77).

[0120] The switch control section 82-1 in a board relays the address-line signal from controller 22-1 as it is till the completion of a transfer (fig. 18 step S78), and returns the discernment bit Sb to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (fig. 18 step S79).

[0121] If the address control section 81-1 in a board cannot secure the above-mentioned band, it relays a transfer failure to controller 22-1 device, and leaves resending etc, to conventional device (fig. 18 step S80).

[0122] Fig. 19 – fig. 23 show actuation when the address control section 81-1 in a board receives a transfer request from the controller 22-1 device via a crossbar switch 5. In this case, the address control section 81-1 in a board investigates the discernment bit which changed to "1" compared with 1 clock front with reference to Memory (C) 81b-1 (fig. 19 steps S91 and S92), and recognizes the port to which data are sent.

[0123] The address control section 81-1 in a board chooses the usable buffer A group 77-1 or the buffer B group 78-1 which becomes clear from this information and the check of a path in use, and instructs a suitable path to the switch control section 82-1 in a board.

[0124] At this time, when 128 bits of data are sent at a time, it is sending a clock to the buffer 72-1, 73-1 and the buffer A group 77-1, or the buffer B group 78-1 of the proceeding paragraph by turns, and step is kept with 256-bit data and it memorizes in the buffer A group 77-1 or the buffer B group 78-1.

[0125] In parallel to this, on the other hand, in order that the address control section 81-1 in a board may make the controller 22-1 by which direct continuation is carried out receive data, a transfer request is sent out. A transfer request is repeated when a controller 22-1 cannot receive data for data from another buffer group because of the transfer middle class.

[0126] When transfer OK comes to the contrary, the address control section 81-1 in a board makes a switch (SW#1) 74-1 changed to an applicable buffer side, starts the clock sending simultaneously to the input buffer 23-1 (refer to fig. 40) conventional device, and makes the data in a buffer incorporate. However, this clock is sent only when 256-bit data exist in an applicable buffer, referring to counter 81d-1 to 81g-1.

[0127] The actuation which sends a control signal is shown in a buffer below from the address control section 81-1 in a board when storing data in the buffer of data division 7-1. when data are transmitted by the transfer partner and 256-bit width, the address control section 81-1 in a board sends a data incorporation signal to the 128-bit buffer of an applicable buffer group and the proceeding paragraph synchronizing with the clock by the side of a crossbar switch 5. Simultaneously, the instruction where counter 81d-1 of

the address control section 81-1 in a board or counter 81e-1 correspond either is counted up.

[0128] Similarly, when having received data by 128 bits, the address control section 81-1 in a board is incorporated to the preceding paragraph buffer which corresponds to the timing of 128 bits of low order received fist. Instruction delivery, while sending a signal to an applicable buffer group to the following clock timing by the side of a crossbar switch 5 and depressing old data in accordance with 128 bits of high orders which are directly visible through the switch 71-1 in a board, and the data for 128 bits of low order which a preceding paragraph buffer has, it incorporates as new data. The instruction where counter 81d-1 of the address control section 81-1 in a board or counter 81e-1 correspond to simultaneously is counted up.

[0129] Conventionally by which direct continuation was carried out from the buffer of data division 7-1, data transfer to the data input section device is performed, after the address control section 81-1 in a board by which direct continuation was carried out receives the signal of the transfer OK from the controller 22-1 to an applicable data block.

[0130] When reference to counter 81d-1 to 81g-1, this data transfer sends the usual clock signal defined beforehand to the clock line of the buffer of the data input section device, when 256-bit data are stored in the buffer group. When there are no 256-bit data in the buffer group, transfer of a clock signal is shelved.

[0131] Namely, when the address control section 81-1 in a board has transmitted data by the transfer partner and 256-bit width. That is, when the discernment bit is changing with Sa=0 →1 and Sb=0 →1 (fig. 19 step S93). Reservation of a→c and a b→d path and modification for a switch (SW#2, #3) 75-1 and the sending-area path of 76-1 are directed to the switch control section 82-1 in a board (fig. 19 step S94).

[0132] The address control section 81-1 in a board will direct to change a switch (SW#1) 74-1 to the buffer A group 77-1 to the switch control section 82-1 in a board, if the transfer request to the controller 22-1 device is OK (fig. 19 step S95) (fig. 19 step S96). The address control section 8-1 in a board will accumulate the transfer request of the address line in the buffer for the addresses for buffer A group 77-1 of Memory (D) 81c-1, if the transfer request to the controller 22-1 device is NG (fig. 19 step S95) (fig. 19 step S99).

[0133] The address control section 81-1 in a board relays address information AAn to corresponding data and coincidence at the controller 22-1 device with reference to record NAAn (n=1,2,3 and 4....) and the clock signal of Memory (D) 81c-1, and transmits the clock of a crossbar switch 5 of operation to the input buffer 23-1 of each time and conventional device as it is (fig. 19 step S97). The address control section 81-1 in a board returns the discernment bits Sa and Sb to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1(fig. 19 step S98).

[0134] Moreover, the address control section 81-1 in a board checks the connection path of port b, when data are transmitted by the transfer partner and 128-bit width (fig. 20 step S100) (when the discernment bit is changing with Sa=0→1) (fig. 20 step S101).

[0135] The address control section 81-1 in a board will direct to change into reservation of a→e and f path to the switch control section 82-1 in a board, if port b is connected to the buffer A group 77-1 (fig. 20 step S102) (fig. 20 step S103).

[0136] The address control section 81-1 in a board will direct to change a switch (SW#1) 74-1 to the buffer B group 78-1 to the switch control section 82-1in a board, if the transfer request to the controller 22-1 device is OK (fig. 20 step S104) (fig. 20 step S105). The address control section 81-1 in a board will accumulate the transfer request of the address line in the buffer for the addresses for buffer B group 78-1 of Memory (D) 81c-1, if the transfer request to the controller 22-1 device is NG (fig. 20 step S104) (fig. 20 step S109).

[0137] If the address control section 81-1 in a board has data of 256-bit width in the buffer B group 78-1 (fig. 20 step S106) record NABn (n=1,2,3 and 4...) and the clock signal of Memory (D) 81c-1 are referred to. Address information Abn is simultaneously relayed to corresponding data at the controller 22-1 device, and the clock of a crossbar switch 5 of operation is transmitted to the input buffer 23-1 of each time and conventional device as it is (fig. 20 step S107). The address control section 81-1 in a board returns the discernment bit Sa to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (fig. 20 step S108).

[0138] The address control section 81-1 in a board directs reservation of a→c and d path, and modification for a switch (SW#2,#3) 75-1 and the sending-area path of 76-1 to the switch control section 82-1 in a board, if port b is not connected to the buffer A group 77-1 (fig. 20 step S102) (fig. 22 step S119).

[0139] The address control section 81-1 in a board will direct to change a switch (SW#1) 74-1 to the buffer A group 77-1 to the switch control section 82-1 in a board, if the transfer request to the controller 22-1 device is OK (fig. 22 step S120) (fig. 22 step S121). The address control section 81-1 in a board will accumulate the transfer request of the address line in the buffer for the addresses for buffer A group 77-1 of Memory (D) 81c-1, if the transfer request to the controller 22-1 device is NG (fig. 22 step S120) (fig. 22 step S125).

[0140] If the address control section 81-1 in a board has data of 256-bit width in the buffer A group 77-1 (fig. 22 step S122) record NAAn (n=1,2,3 and 4...) and the clock signal of Memory (D) 81c-1 are referred to. Address information AAn is simultaneously relayed to corresponding data at the controller 22-1 device, and the clock of a crossbar switch 5 of operation is transmitted to the input buffer 23-1 of each time and conventional device as it is (fig. 22 step S123). The address control section 81-1 in a board returns the discernment bit Sa to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (fig. 22 step S124).

[0141] The address control section 81-1 in a board will direct to change into reservation of a→e and f path to the switch control section 82-1 in a board, if port a is connected to the buffer A group 77-1 when data are transmitted by the transfer partner and 128-bit width (fig. 21 step S110) (when the discernment bit is changing with Sb=0→1) (fig. 21 step S111) (fig. 21 step S112).

[0142] The address control section 81-1 in a board will direct to change a switch (Sw#1) 74-1 to the buffer B group 78-1 to the switch control section 82-1 in a board, if the transfer request to the controller 22-1 device is OK (fig. 21 step S113) (fig. 21 step S114). The address control section 81-1 in a board will accumulate the transfer request of the address line in the buffer for the addresses for buffer B group 78-1 of Memory (D) 81c-1, if the transfer request to the controller 22-1 device is NG (fig. 21 step S113) (fig. 21 step S118).

[0143] If the address control section 81-1 in a board has data of 256-bit width in the buffer B group 78-1 (fig. 21 step S115) record NABn (n=1,2,3 and 4...) and the clock signal of Memory (D) 81c-1 are referred to. Address information Abn is relayed to corresponding data and coincidence at the controller 22-1 device, and the clock of a crossbar switch 5 of operation is transmitted to the input buffer 23-1 of each time and device as it is (fig. 21 step S116). The address control section 81-1 in a board returns the discernment bit Sb to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (fig. 21 step S117).

[0144] The address control section 81-1 in a board directs reservation of a→e and d path, and modification for a switch (SW#2,#3) 75-1 and the sending-area path of 76-1 to the switch control section 82-1 in a board, if port a is not connected to the buffer A group 77-1 (fig. 21 step S111) (fig. 23 step S126).

[0145] The address control section 81-1 in a board will direct to change a switch (SW#1) 74-1 to the buffer A group 77-1 to the switch control section 82-1 in a board, if the transfer request to the controller 22-1 device is OK (fig. 23 step S127) (fig. 23 step S128). The address control section 81-1 in a board will accumulate the transfer request of the address line in the buffer for the addresses for buffer A group 77-1 of Memory (D) 81c-1 if the transfer request to the controller 22-1 device is NG (fig. 23 step S127) (fig. 23 step S132).

[0146] If the address control section 81-1 in a board has data of 256-bit width in the buffer A group 77-1 (fig. 23 step S129) record NAAn (n=1,2,3 and 4...) and the clock signal of Memory (D) 81c-1 are referred to. Address information AAn is relayed to corresponding data and coincidence at the controller 22-1 device, and the clock of a crossbar switch 5 of operation is transmitted to the input buffer 23-1 of each time and conventional device as it is (fig. 23 step S130). The address control section 81-1 in a board returns the discernment bit Sb to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (fig. 23 step S131).

[0147] Fig. 24 is a figure in which showing a division in the case of the data transfer in the crossbar switch device 1 by one example of this invention. In drawing, C1 shows the case where a 256-bit band can be secured in case 256-bit data are transmitted to a 256-bit port, C2 shows the case where a 128-bit band can be secured in case 256-bit data are transmitted to a 256-bit port, and in case C3 transmits 256 bit data to a 256 bit port, it shows the case where a band is not securable.

[0148] C4 shows the case where a 128-bit band can be secured in case 128-bit data are transmitted to a 256-bit port, and in case C5 transmits 128-bit data to a 256-bit port, it shows the case where a band is not securable.

[0149] C6 shows the case where a 128-bit band can be secured in case 256-bit data are transmitted to a 128-bit port, and in case C7 transmits 256-bit data to a 128-bit port, it shows the case where a band is not securable.

[0150] C8 shows the case where a 128-bit band can be secured in case 128-bit data are transmitted to a 128-bit port, and in case C9 transmits 128-bit data to a 128-bit port, it shows the case where a band is not securable.

[0151] In case fig. 25 transmits the 256-bit data based on one example of this invention to a 256-bit port, it is a figure showing actuation of a requestor side when a 256-bit band is securable (in the case of C1), and in case fig. 26 transmits the 256-bit data based on one example of this invention to a 256-bit port, if is a figure showing the actuation by the side of supply when a 256-bit band is securable (in the case of C1).

[0152] In case fig. 27 transmits the 256-bit data based on one example of this invention to a 256-bit port, it is a figure showing actuation of a requestor side when a 128-bit band is securable (in the case of C2), and in case fig. 28 transmits the 256-bit data based on one example of this invention to a 256-bit port, it is a figure showing the actuation by the side of supply when a 128-bit band is securable in (in the case of C2).

[0153] In case fig. 29 transmits the 256-bit data based on one example of this invention to a 256-bit port, it is a figure showing actuation of a requestor side when a band is not securable (in the case of C3), and in case fig. 30 transmits the 256-bit data based on one example of this invention to a 256-bit port, it is a figure showing the actuation by the side of supply when a band is not securable (in the case of C3).

[0154] In case fig. 31 transmits the 128-bit data based on one example of this invention to a 256-bit port, it is a figure showing actuation of a requestor side when a 128-bit band is securable (in the case of C4), and in case fig. 32 transmits the 128-bit data based on one example of this invention to a 256-bit port, it is a figure showing the actuation by the side of supply when a 128-bit band is securable (in the case of C4).

[0155] In case fig. 33 transmits the 128-bit data based on one example of this invention to a 256-bit port, it is a figure showing actuation of a requestor side when a band is not securable (in the case of C5), and in case fig. 34 transmits the 128-bit data based on one

example of this invention to a 256-bit port, it is a figure showing the actuation by the side of supply when a band is not securable (in the case of C5).

[0156] In case fig. 35 transmits the 256-bit data based on one example of this invention to a 128-bit port, it is a figure showing actuation of a requestor side when a 128-bit band is securable (in the case of C6), and in case fig. 36 transmits the 256-bit data based on one example of this invention to a 128-bit port, it is a figure showing the actuation by the side of supply when a 128-bit band is securable (in the case of C6).

[0157] In case fig. 37 transmits the 256-bit data based on one example of this invention to a 128-bit port, it is a figure showing actuation of a requestor side when a band is not securable (in the case of C7), and in fig. 38 transmits the 256-bit data based on one example of this invention to a 128-bit port, it is a figure showing the actuation by the side of supply when a band is not securable (in the case of C7).

[0158] With reference to these fig. 1- fig. 11 and fig. 24-fig. 38, the data transfer using the crossbar switch device 1 by one example of this invention is explained. In addition, in the case of C8 and C9, which are shown in fig. 24, it is the same environment as the conventional device, and since it is obvious, the actuation is not explained.

[0159] First, in case 256-bit data are transmitted to a 256-bit port, when a 256-bit band can be secured (in the case of C1), if there is a transfer request from the controller 22-1 device when the discernment bits Sa and Sb are "0" in both requestor sides (processing C1-1) the address control section 81-1 in a board makes the discernment bits Sa and Sb both "1", and sends out a transfer request (processing C1-2(Sa=0→1, Sb=0→1)). Here, in both supply sides, the discernment bits Sa and Sb are "0" at processing C-1 and the time of C-2.

[0160] Then, the crossbar switch side address control section 61-1 of a requestor side sends out a transfer request to the two address lines of a communications partner, if the discernment bits Sa and Sb become both "1". The crossbar switch side address control section 61-1 by the side of supply detects the transfer request of the two address lines. At this time, in a requestor side, the discernment bits Sa and Sb are "1" and supply sides,, and are "0" (processing C 1-3).

[0161] Since the discernment bits Sa and Sb are "0", both the crossbar switch side address control section 61-1 by the side of supply answer transfer OK to both two address lines, both make the discernment bits Sa and Sb simultaneously "1" (Sa=0→1, Sb=0→1), and send out a transfer request to a board. Then, the address control section 81-1 in a board by the side of supply directs routing of a→c and b→d to the switch control section 82-1 in a board (processing C1-4).

[0162] The address control section 81-1 in a board by the side of supply transmits a transfer request to the controller 22-1 device. If transfer OK is checked from both two address lines, the crossbar switch side address control section 61-1 of a requestor side

will both consider the discernment bits Sa and Sb as "1", and will transmit transfer OK to a board (processing C 1-5).

[0163] The switch control section 82-1 in a board of a requestor side directs routing of a→c and b→d to the switch control section 82-1 in a board, and directs to make a switch (SW#2, SW#3) 75-1 and 76-1into a sending area (processing C 1-6).

[0164] The switch control section 82-1 in a board of a requestor side sends out data, if a directed setup is performed. The switch control section 82-1 in a board by the side of supply receives the sent data by the buffer A group 77-1 (processing C 1-7).

[0165] The data input section device incorporates the address control section 81-1 in a board by the side of supply from a buffer group, and it does not have inner data, or checks incorporation termination (processing C1-8).

[0166] The address control section 81-1 in a board by the side of supply sends the address to the controller device after a check. The crossbar switch side address control section 61-1 directs to set a switch (SW#1) 74-1 as the buffer A group 77-1 (processing C 1-9).

[0167] The address control section 81-1 in a board of a requestor side returns the discernment bits Sa and Sb to "0" after the completion of sending out (Sa=1→0, Sb=1→0), and the address control section 81-1 in a board by the side of supply returns the discernment bits Sa and Sb to "0" after the completion of a transfer (refer to fig. 25 and fig. 26). (Sa=1→0, Sb=1→0) (processing C 1-10).

[0168] In case 256-bit data are transmitted to a 256-bit port, when a 128-bit band can be secured (in the case of C2), a requestor-side and supply side performs the above-mentioned processing C 1-1 to C1-3.

[0169] After that, the crossbar switch side address control section 61-1 by the side of supply answers transfer OK to the address line of the side which recognizes and is empty in seeing the discernment bits Sa and Sb and port a or port b using it, sets the discernment bits Sa and Sb corresponding simultaneously to "1" (Sa=0→1 or Sb=0→1), and sends out a transfer request to a board (processing C 2-1).

[0170] The address control section 81-1 in a board by the side of supply directs to secure the path to a buffer group securable from the port secured to the switch control section 82-1 in a board. If transfer OK is checked from one side of the two address lines, the crossbar switch side address control section 61-1 of a requestor side will set to "0" the discernment bits Sa and Sb of the direction to which transfer OK did not come (0 1→1, 1→0, or 1), and will transmit transfer OK to a board (processing C 2-2).

[0171] The address control section 81-1 in a board of a requestor side transmits transfer OK to the controller 22-1 device, and directs to make a switch (SW#2, SW#3) 75-1 and 76-1 the switch control section 82-1 in a board at a sending area (processing C 2-3).

[0172] The switch control section 82-1 in a board of a requestor side is c→a to the switch control section 82-1 in a board or b, d→a or routing of b is directed and new data are required once of two clocks at the output section device. A transfer request is transmitted to the controller 22-1 device, the switch control section 82-1 in a board switches switch (SW#11) 71a-1 or switch (SW#12) 71b-1 for every clock, and the address control section 81-1 in a board by the side of supply secures the path which sends data to the height order lower bit of a buffer group in order (processing C 2-4).

[0173] The switch control section 82-1 in a board of a requestor side sends out data, if a directed setup is performed. The switch control section 82-1 in a board by the side of supply receives the sent data by the buffer A group 77-1 or the buffer B group 78-1 (processing C 2-5). Henceforth, a requestor-side and supply side performs the above-mentioned processing C 1-8 to C 1-10 (refer to fig. 27 and fig. 28).

[0174] In case 256-bit data are transmitted to a 256-bit port, when a band cannot be secured (in the case of C3), a requestor-side and supply side performs the above-mentioned processing C 1-1 to C 1-3.

[0175] After that, the crossbar switch side address control section 61-1 by the side of supply recognizes that see the discernment bits Sa and Sb and port a and port bare using it, and answers a band secured improper signal (processing C 3-1).

[0176] The crossbar switch side address control section 61-1 of a requestor side transmits a band secured improper signal to a board as it is, and sets both the discernment bits Sa and Sb to "0" (processing C 3-2). (Sa=1→0, Sb=1→0)

[0177] The address control section 81-1 in a board of a requestor side transmits a band secured improper signal to the controller 22-1 device (processing C 3-3). Henceforth, he leaves it to the resending demand of the controller 22-1 device. When the cause of resending in device receipt-side is taking out, it is requiring even the controller 22-1 device by the side of receipt, and is usable with the method (refer to fig. 29 and fig. 30).

[0178] In case 128-bit data are transmitted to a 256-bit port, when a 128-bit band can be secured (in the case of C4), the crossbar switch side address control section 61-1 of a requestor side sends out a transfer request to either of the two address lines by the side of receipt from the only address line. The crossbar switch side addresses control section 61-1 by the side of supply detects one transfer request of the two address lines (processing C 4-1).

[0179] The discernment bit of the side which checks that the crossbar switch side address control section 61-1 by the side of supply saw the discernment bits Sa and Sb, and port a and either of the b are empty, and replies transfer OK from the address line of empty one of ports is set to "1" (processing C 4-2).

[0180] If transfer OK is checked from one side of the two address lines, the crossbar switch side address control section 61-1 of a requestor side will transmit transfer OK to a board, and will change the data receiver's address into a port with a reply. The address control section 81-1 in a board transmits transfer OK to the controller 22-1 device (processing C 4-3).

[0181] Then, in a supply side, the above-mentioned processing C 2-2 to C 2-5 and C 1-8 to 1-10 are performed. Moreover, in a requestor side, if processing C 4-3 is performed, the signal and data from a controller 22-1 device will be outputted as it is (refer to fig. 31 and fig. 32).

[0182] In case 128-bit data are transmitted to a 256-bit port, when a band cannot be secured (in the case of C5), the crossbar switch control section 61-1 of a requestor side sends out a transfer request to one address line of the receipt sides from the only address line. The crossbar switch side address control section 61-1 by the side of supply detects one transfer request of the two address lines (processing C 5-1).

[0183] The crossbar switch side address control section 61-1 by the side of supply recognizes that the discernment bits Sa and Sb and port a and port b are using it, and answers a band secured improper signal (processing C 5-2).

[0184] The crossbar switch side address control section 61-1 of a requestor side transmits a band secured improper signal to a board as it is (processing C 5-3). Henceforth, he leaves it to the resending demand of the controller 22-1 device. When the cause of resending device receipt-side is taking out, it is requiring even the controller 22-1 device by the side of receipt, and is useable with the method (refer to fig. 33 and fig. 24).

[0185] In case 256-bit data area transmitted to a 128-bit port, when a 128-bit band can be secured (in the case of C6), the crossbar switch side address control section 61-1 of a requestor side sends out a transfer request to either of the two address lines. The crossbar switch side address control section 61-1 by the side of supply detects a transfer request from the address line (processing C 6-1).

[0186] The crossbar switch side address control section 61-1 by the side of supply replies transfers OK to the address line in a sender's port. The crossbar switch side address control section 61-1 of a requestor side will transmit transfer OK to a board, if transfer OK is checked from the address line (processing C 6-2).

[0187] Then, in a requestor side, the above-mentioned processing C 2-3 to C2-5, and C 1-8 to 1-10 are performed. Moreover, in a supply side, if processing C 6-2 is performed, a signal and data will be inputted into the controller 22-1 device as it is (refer to fig. 35 and fig. 36).

[0188] In case 256-bit data are transmitted to a 128-bit port, when a band cannot be secured (in case of C7), the crossbar switch side address control section 61-1 of a requestor side sends out a transfer request from either of the two address lines. The

crossbar switch side address control section 61-1 by the side of supply detects a transfer request from the address line (processing C 7-1).

[0189] The crossbar switch side address control section 61-1 by the side of supply replies a band secured improper signal to the address lines with a sender's port. The crossbar switch side address control section 61-1 of a requestor side will transmit a band secured improper signal to a board, if a band secured improper signal is checked from the address line (processing C 7-2).

[0190] Henceforth, he leaves it to the resending demand of the controller 22-1 device. When the cause of resending in device receipt-side is taking out, it is requiring even the controller 22-1 device by the side of receipt, and is usable with the method (refer to fig. 37 and fig. 38).

[0191] Thus, since it has the switch and controller which distribute data to two input buffers and this in the board which can receive data with wide width, it can transmit to the board and simultaneously from which two data width differs.

[0192] Moreover, since it has the switch and controller which distribute data to the point of the output buffer of the board which can send data with wide width, if the port equivalent to half data width is intact even if data are under transfer, another data transfer can be performed.

[0193] Furthermore, since the address line, a 2 bits discernment bit, and one 1-bit a and b port discernment line are used instead of preparing 2 sets of address line, physical size of a connection part can be made small and it can realize cheaply.

[0194] Since common use is attained further again, without the data line/address line being dependent on the bus width communication partner, it is cheaply realizable rather than it prepares two or more ports doubled with the data width of a communication partner.

[0195]
[Effects of the Invention] As explained above, according to this invention, it has two or more ports of the same data width where two or more boards are connected. In the data width good transformation crossbar switch device which connects between two or more boards through two or more ports which share an address signal by performing the communication with other boards through the port which has empty ports where a board with wide data width is connected, in case the data width of the boards which communicate differs, it is effective in the ability for the data width connected to the crossbar switch not to be connected, and communicate to the data width of a partner's port in a large port, also during the communication with the port where data width is narrow.

[Brief Description of the Drawings]

[Fig. 1] It is the block diagram showing the configuration of the crossbar switch device by one example of this invention.

[Fig. 2] It is the block diagram showing the configuration of the crossbar switch side I/O section of fig.1.

[Fig. 3] It is the block diagram showing the configuration of the data division of fig. 1.

[Fig. 4] It is the block diagram showing the configuration of the address control section of fig. 1.

[Fig. 5] It is the block diagram showing the configuration of the switch in a board of fig. 3.

[Fig. 6] (a) And (b) are drawings showing the configuration of the switch shown in fig. 3 and fig. 5.

[Fig. 7] It is the block diagram showing the configuration of a crossbar switch side address control section shown in fig. 2.

[Fig. 8] Drawing in which (a) shows the contents of storage of the memory (A) of fig. 7, and (b) are drawings showing the contents of storage of the memory (B) of fig. 7.

[Fig. 9] It is the block diagram showing the configuration of the address control section in a board of fig. 4.

[Fig. 10] Drawing in which (a) shows the contents of storage of the memory (c) of fig. 9, and (b) are drawings showing the contents of storage of the memory (d) of fig. 9.

[Fig. 11] It is drawing showing control of the switch of fig. 3 by the switch control section in a board of fig. 4 and fig. 5.

[Fig. 12] It is the flow chart, which shows the actuation of a crossbar switch side address control section shown in fig. 2 and fig. 7.

[Fig. 13] It is the flow chart, which shows the actuation of a crossbar switch side address control section shown in fig. 2 and fig. 7.

[Fig. 14] It is the flow chart, which shows the actuation of a crossbar switch side address control section shown in fig. 2 and fig. 7.

[Fig. 15] It is the flow chart, which shows the actuation of a crossbar switch side address control section shown in fig. 2 and fig. 7.

[Fig. 16] It is the flow chart, which shows the actuation of the address control section in a board shown in fig. 4 and fig. 9.

[Fig. 17] It is the flow chart, which shows the actuation of the address control section in a board shown in fig. 4 and fig. 9.

[Fig. 18] It is the flow chart, which shows the actuation of the address control section in a board shown in fig. 4 and fig. 9.

[Fig. 19] It is the flow chart, which shows the actuation of the address control section in a board shown in fig. 4 and fig. 9.

[Fig. 20] It is the flow chart, which shows the actuation of the address control section in a board shown in fig. 4 and fig. 9.

[Fig. 21] It is the flow chart, which shows the actuation of the address control section in a board shown in fig. 4 and fig. 9.

[Fig. 22] It is the flow chart, which shows the actuation of the address control section in a board shown in fig. 4 and fig. 9.

[Fig. 23] It is the flow chart, which shows the actuation of the address control section in a board shown in fig. 4 and fig. 9.

[Fig. 24] It is drawing in which showing a division in the case of the data transfer in the crossbar switch device by one example of this invention.

[Fig. 25] In case the 256-bit data based on one example of this invention are transmitted to a 256-bit port, it is a drawing showing actuation of a requestor side when a 256-bit band is securable.

[Fig. 26] In case the 256-bit data based on one example of this invention are transmitted to a 256-bit port, it is a drawing showing actuation by the side of supply when a 256-bit band is securable.

[Fig. 27] In case the 256-bit data based on one example of this invention are transmitted to a 256-bit port, it is a drawing showing actuation of a requestor side when a 128-bit band is securable.

[Fig. 28] In case the 256-bit data based on one example of this invention are transmitted to a 256-bit port, it is a drawing showing actuation by the side of supply when a 128-bit band is securable.

[Fig. 29] In case the 256-bit data based on one example of this invention are transmitted to a 256-bit port, it is a drawing showing actuation of a requestor side when a band is not securable.
[Fig. 30] In case the 256-bit data based on one example of this invention are transmitted to a 256-bit port, it is a drawing showing actuation by the side of supply when a band is not securable.

[Fig. 31] In case the 128-bit data based on one example of this invention are transmitted to a 256-bit port, it is a drawing showing actuation of a requestor side when a 128-bit band is securable.

[Fig. 32] In case the 128-bit data based on one example of this invention are transmitted to a 256-bit port, it is a drawing showing actuation by the side of supply when a 128-bit band is securable.

[Fig. 33] In case the 128-bit data based on one example of this invention are transmitted to a 256-bit port, it is a drawing showing actuation of a requestor side when a band is not securable.

[Fig. 34] In case the 128-bit data based on one example of this invention are transmitted to a 256-bit port, it is a drawing showing actuation by the side of supply when a band is not securable.

[Fig. 35] In case the 256-bit data based on one example of this invention are transmitted to a 128-bit port, it is a drawing showing actuation of a requestor side when a 128-bit band is securable.

[Fig. 36] In case the 256-bit data based on one example of this invention are transmitted to a 128-bit port, it is a drawing showing actuation by the side of supply when a 128-bit band is securable.

[Fig. 37] In case the 256-bit data based on one example of this invention are transmitted to a 128-bit port, it is a drawing showing actuation of a requestor side when a band is not securable.

[Fig. 38] In case the 256-bit data based on one example of this invention are transmitted to a 128-bit port, it is a drawing showing actuation by the side of supply when a band is not securable.

[Fig. 39] It is the block diagram showing the configuration of the processor board of fig. 39.

[Description of Notations]

1 Crossbar switch device

2-1, 2-2 processor board

3-1, 3-2 memory board
4-1 to 4-4 I/O board

5 Crossbar Switch

6-1 to 6-4 Crossbar switch side I/O section

7-1 to 7-4 Data division

8-1 to 8-4 Address control section

61-1 Crossbar switch side address control section

61a-1 Controller

61b-1 Memory (A)

61c-1 Memory (B)

71-1 Switch in Board

72-1, 73-1 Buffer

74-1 to 76-1, 71a-1 to 71j-1 Switch

77-1 Buffer A group

78-1 Buffer B group

81-1 Address control section in board

81a-1 Controller

81b-1 Memory (C)

81c-1 Memory (D)

81d-1 to 81g-1 Counter

82-1 Switch control section in board

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FACSIMILE TRANSMITTAL SHEET

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Mr. Roger D. Greer	Christopher E. Lee / AU 2112
FAX NUMBER: 312-360-9315	DATE: September 1, 2004
COMPANY: Attorney Agent for Applicant	TOTAL NO. OF PAGES INCLUDING COVER: 26
PHONE NUMBER: 312-360-0080	APPLICATION SERIAL NUMBER: 10/044,401
RE: Yokoyama's Translated Version	ATTORNEY DOCKET NUMBER: 10016664-1

☐ URGENT ☑ FOR REVIEW ☐ PLEASE COMMENT ☐ PLEASE REPLY ☐ PLEASE RECYCLE

NOTES/COMMENTS:

The Examiner refers to Yokoyama et al. [JP 411296473 A] reference as a prior art for the claim rejections in the Non-Final Office Action mailed on 16th of June 2004, and it is referred to the original copy of foreign reference in foreign language (i.e., Japanese). Here, the Examiner provides a machine translated copy of the reference for the convenience of the Applicants. However, the Examiner cautions the Applicants that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely.

Thank you,

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CLAIMS

[Claim(s)]
[Claim 1] It has two or more ports of the same data width of face where two or more boards are connected, respectively. It is data width-of-face adjustable mold crossbar switch equipment which connects between said two or more boards through said two or more ports. Data width-of-face adjustable mold crossbar switch equipment characterized by constituting so that the communication link with other boards may be performed through the port which has **ed of the ports where a board with said wide data width of face is connected, in case the data width of face of the boards which communicate differs.
[Claim 2] It has two or more ports of the same data width of face where two or more boards are connected, respectively. It is data width-of-face adjustable mold crossbar switch equipment which connects between said two or more boards through said two or more ports. A detection means to detect the port which has **ed of the ports where a board with said wide data width of face is connected in case the data width of face of the boards which communicate differs, Data width-of-face adjustable mold crossbar switch equipment characterized by having a means to perform the communication link with other boards through the port detected with said detection means.
[Claim 3] Data width-of-face adjustable mold crossbar switch equipment according to claim 2 characterized by constituting so that said two or more ports may be assigned to a board with said wide data width of face.
[Claim 4] Said detection means is data width-of-face adjustable mold crossbar switch equipment according to claim 3 characterized by constituting so that the port which is vacant out of two or more ports assigned to the board with said wide data width of face may be detected.
[Claim 5] Said detection means is data width-of-face adjustable mold crossbar switch equipment according to claim 3 or 4 characterized by constituting so that a port in use [of said two or more ports] may be pinpointed based on two or more address information from the ports of each assigned to the board with said wide data width of face.
[Claim 6] For said detection means, claim 3 to claim 5 characterized by to include a storage means memorize the information on the port assigned to two or more of said boards of each, and a maintenance means hold the information which pinpoints the ports of each which were assigned to two or more of said boards of each, and which were assigned to the board and the board concerned of a communications partner for every port is data width-of-face adjustable mold crossbar switch equipment of a publication either.
[Claim 7] Claim 2 to claim 6 characterized by including 1st and 2nd storing means to store the data with which said data width of face is delivered and received between boards and communications partners concerned with the data width of face of a large board in the board concerned is data width-of-face adjustable mold crossbar switch equipment of a publication either.
[Claim 8] Claim 2 to claim 7 characterized by including a setting-out means to set up the I/O path of the data delivered and received between boards and communications partners with said wide data width of face in the board concerned is data width-of-face adjustable mold crossbar switch equipment of a publication either.

[Claim 9] It has two or more ports of the same data width of face where two or more boards are connected, respectively. It is the connection method of the data width-of-face adjustable mold crossbar switch equipment which connects between said two or more boards through said two or more ports. The connection method of the data width-of-face adjustable mold crossbar switch equipment characterized by performing the communication link with other boards through the port which has **ed of the ports where a board with said wide data width of face is connected when the data width of face of the boards which communicate differs.
[Claim 10] It has two or more ports of the same data width of face where two or more boards are connected, respectively. It is the connection method of the data width-of-face adjustable mold crossbar switch equipment which connects between said two or more boards through said two or more ports. The step which detects the port which has **ed of the ports where a board with said wide data width of face is connected in case the data width of face of the boards which communicate differs, The connection method of the data width-of-face adjustable mold crossbar switch equipment characterized by having the step which performs the communication link with other boards through the detected port.
[Claim 11] The connection method of the data width-of-face adjustable mold crossbar switch equipment according to claim 10 characterized by assigning said two or more ports to a board with said wide data width of face.
[Claim 12] The step which detects said vacant port is the connection method of the data width-of-face adjustable mold crossbar switch equipment according to claim 11 characterized by constituting so that the port which is vacant out of two or more ports assigned to the board with said wide data width of face may be detected.
[Claim 13] The step which detects said vacant port is the connection method of the data width-of-face adjustable mold crossbar switch equipment according to claim 11 or 12 characterized by pinpointing a port in use [of said two or more ports] based on two or more address information from the ports of each assigned to the board with said wide data width of face.
[Claim 14] The step which detects said vacant port A storage means to memorize the information on the port assigned to said two or more boards of each, So that said vacant port may be detected using a maintenance means to hold the information which pinpoints the ports of each which were assigned to said two or more boards of each, and which were assigned to the board and the board concerned of a communications partner for every port Claim 11 to claim 13 characterized by carrying out is the connection method of the data width-of-face adjustable mold crossbar switch equipment of a publication either.
[Claim 15] Claim 11 to claim 14 characterized by storing the data delivered and received between boards and communications partners concerned by one side of the 1st and 2nd storing means by which said data width of face has the data width of face of a large board is the connection method of the data width-of-face adjustable mold crossbar switch equipment of a publication either.
[Claim 16] Claim 10 to claim 15 characterized by including the step which sets up the I/O path of the data delivered and received between boards and communications partners with said wide data width of face is the connection method of the data width-of-face adjustable mold crossbar switch equipment of a publication either.
[Claim 17] It has two or more ports of the same data width of face where two or more boards are connected, respectively. It is the record medium which recorded the connection control program for making the processing which connects between said two or more boards through said two or more ports perform to a processor. Said connection control program is the record medium which recorded the connection control program characterized by making the communication link with other boards perform to said processor through the port which has **ed of the ports where a board with said wide data width of face is connected in case the data width of face of the boards which communicate differs.
[Claim 18] It has two or more ports of the same data width of face where two or more boards are connected, respectively. It is the record medium which recorded the connection control program for making the processing which connects between said two or more boards through said two or more ports perform to a processor. Said connection control program makes the port which has **ed of the ports

where a board with said wide data width of face is connected to it in case the data width of face of the boards which communicate differs in said processor detect. The record medium which recorded the connection control program characterized by making the communication link with other boards perform through the detected port.

[Claim 19] Said connection control program is the record medium which recorded the connection control program according to claim 18 characterized by making the port which is vacant out of two or more ports assigned to the board with said wide data width of face detect in case said processor is made to detect said vacant port.

[Claim 20] Said connection control program is the record medium which recorded the connection control program according to claim 18 or 19 characterized by making a port in use [of said two or more ports] pinpoint based on two or more address information from the ports of each assigned to the board with said wide data width of face in case said processor is made to detect said vacant port.

[Claim 21] A storage means to memorize the information on the port assigned to said two or more boards of each in case said connection control program makes said processor detect said vacant port,

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the crossbar switch equipment which connects between ports with especially different data width of face about the record medium which recorded the control program on data width-of-face adjustable mold crossbar switch equipment and its connection method list.
[0002]
[Description of the Prior Art] Conventionally, in this kind of crossbar switch equipment, as shown in drawing 39 , the processor board (#1-#3) 2-1 to 2-3, the memory board (#1-#3) 3-1 to 3-3, and the I/O (I/O) board (#1-#6) 4-1 to 4-6 are mutually connected through a crossbar switch 5.
[0003] In this case, it has data width of face different, respectively in the processor board (#1-#3) 2-1 to 2-3, the memory board (#1-#3) 3-1 to 3-3, and the I/O (I/O) board (#1-#6) 4-1 to 4-6. That is, the crossbar switch 5 has connected between the ports of different data width of face.
[0004] Here, as shown in the processor board (#1) 2-1 at drawing 40 , the processor 21-1, the controller 22-1, the input buffer 23-1, and the output buffer 24-1 are carried, and they are mutually connected by bus 200-1 in a board.
[0005] In addition, although not illustrated, it has the same composition as other processor boards (#2, #3) 2-2 and the processor board (#1) 2-1 of the above [2-3]. Moreover, although not illustrated like the above, the memory board (#1-#3) 3-1 to 3-3 and the I/O (I/O) board (#1-#6) 4-1 to 4-6 also have the same composition as the above-mentioned processor board (#1) 2-1 except carrying memory and I/O instead of a processor 21-1.
[0006] Above crossbar switch equipment is performing the communication link in the ports of the same data width of face because a controller 22-1 controls an input buffer 23-1 and an output buffer 24-1.
[0007]
[Problem(s) to be Solved by the Invention] Although between the ports of the data width of face from which a crossbar switch differs is connected with the conventional crossbar switch equipment mentioned above, if between different data width of face is connected with a crossbar switch, and it is communicating between the ports where data width of face is narrow, the transfer between the ports where data width of face is widc cannot be performed.
[0008] Moreover, although the possibility of a concurrent access demand of the parts of memory etc. can solve the above-mentioned problem by preparing the large transfer path of data width of face independently about a high part, in that case, a utilization ratio will become low and will cause the increment in the amount of hardware.
[0009] Furthermore, although the above-mentioned technical problem is also solvable by giving the port where two or more data width of face is narrow on two or more same board instead of being the port where data width of face is wide, two or more the address lines and the controllers which connect an applicable board and a crossbar switch will also be needed, and will cause large buildup of the amount of hardware.

[0010] Then, it is in the object of this invention offering the record medium which recorded the control program on the data width-of-face adjustable mold crossbar switch equipment with which the data width of face which canceled the above-mentioned trouble and was connected to the crossbar switch cannot be concerned, and can communicate to the data width of face of a phase hand's port in a large port also during the communication link with the port where data width of face is narrow, and its connection method list.

[0011]

[Means for Solving the Problem] The data width-of-face adjustable mold crossbar switch equipment by this invention It has two or more ports of the same data width of face where two or more boards are connected, respectively. It is data width-of-face adjustable mold crossbar switch equipment which connects between said two or more boards through said two or more ports. In case the data width of face of the boards which communicate differs, it constitutes so that the communication link with other boards may be performed through the port which has **ed of the ports where a board with wide data width of face is connected.

[0012] Other data width-of-face adjustable mold crossbar switch equipments by this invention It has two or more ports of the same data width of face where two or more boards are connected, respectively. It is data width-of-face adjustable mold crossbar switch equipment which connects between said two or more boards through said two or more ports. It has a detection means to detect the port which has **ed of the ports where a board with wide data width of face is connected in case the data width of face of the boards which communicate differs, and a means to perform the communication link with other boards through the port detected with said detection means.

[0013] The connection method of the data width-of-face adjustable mold crossbar switch equipment by this invention It has two or more ports of the same data width of face where two or more boards are connected, respectively. It is the connection method of the data width-of-face adjustable mold crossbar switch equipment which connects between said two or more boards through said two or more ports. In case the data width of face of the boards which communicate differs, it is made to perform the communication link with other boards through the port which has **ed of the ports where a board with wide data width of face is connected.

[0014] The connection method of other data width-of-face adjustable mold crossbar switch equipments by this invention It has two or more ports of the same data width of face where two or more boards are connected, respectively. It is the connection method of the data width-of-face adjustable mold crossbar switch equipment which connects between said two or more boards through said two or more ports. It has the step which detects the port which has **ed of the ports where a board with wide data width of face is connected in case the data width of face of the boards which communicate differs, and the step which performs the communication link with other boards through the detected port.

[0015] The record medium which recorded the connection control program by this invention It has two or more ports of the same data width of face where two or more boards are connected, respectively. It is the record medium which recorded the connection control program for making the processing which connects between said two or more boards through said two or more ports perform to a processor. Said connection control program is making the communication link with other boards perform to it through the port which has **ed of the ports where a board with wide data width of face is connected, in case the data width of face of the boards which communicate differs in said processor.

[0016] The record medium which recorded other connection control programs by this invention It has two or more ports of the same data width of face where two or more boards are connected, respectively. It is the record medium which recorded the connection control program for making the processing which connects between said two or more boards through said two or more ports perform to a processor. In case the data width of face of the boards which communicate differs in said processor, said connection control program makes it detect the port which has **ed of the ports where a board with wide data width of face is connected, and is making the communication link with other boards perform to it through the detected port.

[0017] That is, the data width-of-face adjustable mold crossbar switch equipment of this invention can

be made to perform the communication link with other boards in the port as for which the near board in which data width of face has a large port was vacant, in case the data width of face of the boards which communicate differs.
[0018] Namely, the switch in a board is formed and data are distributed for every communications partner. Moreover, in addition to the switch in a board, two buffer groups in which data width of face has the same data width of face as the maximum data width of face of a large port are prepared in data division, and the data which were able to be distributed with the switch in a board are saved respectively. The switch control section in a board is directed on each switch (SW) in which the path of a I / O data was prepared by the switch in a board based on the signal from the address control section in a board.
[0019] As mentioned above, data width of face becomes possible [carrying out the division activity of the port to the crossbar switch in a board with a large port] by having the structure which saves two data, and the controlling mechanism which distributes data.
[0020]
[Embodiment of the Invention] Next, one example of this invention is explained with reference to a drawing. Drawing 1 is the block diagram showing the configuration of the crossbar switch equipment by one example of this invention. In drawing, crossbar switch equipment 1 is equipped with a crossbar switch 5 and the crossbar switch side I/O section 6-1 to 6-4, and data division 7-1 to 7-4 and the address control section 8-1 to 8-4 are arranged corresponding to the processor board 2-1 with wide data width of face (#1, #2), 2-2 and the memory board (#1, #2) 3-1, and 3-2 each.
[0021] The crossbar switch 5 had 12 128-bit ports, connected to the 128-bit port the I/O (I/O) board (#1-#4) 4-1 to 4-4 whose data width of face is 128-bit width of face as it was, and has connected to two 128-bit ports the processor board 2-1 whose data width of face is 256-bit width of face, 2-2 and the memory board 3-1, and 3-2, respectively.
[0022] That is, crossbar switch equipment 1 is connected through the crossbar switch side I/O section 6-1 to 6-4 by which the processor board 2-1, 2-2 and the memory board 3-1, and 3-2 were connected to two ports of a crossbar switch 5.
[0023] By the crossbar switch side I/O section 6-1 to 6-4, above-mentioned data division 7-1 to 7-4, and the above-mentioned address control section 8-1 to 8-4 In case the data width of face of the boards which communicate differs (for example, the processor board 2-1, 2-2 and the memory board 3-1, and 3-2 have data width of face larger than the I/O board (#1-#4) 4-1 to 4-4) It can be made to perform the communication link with other boards in the port as for which the near board in which data width of face has a large port was vacant.
[0024] That is, the switch in a board (not shown) is formed in data division 7-1 to 7-4, and data are distributed for every communications partner. Moreover, in addition to the switch in a board, two buffer groups (not shown) of 256-bit width of face are prepared in data division 7-1 to 7-4, and the data which were able to be distributed with the switch in a board are saved by two buffer groups in each.
[0025] The switch control section in a board (not shown) prepared in the address control section 8-1 to 8-4 is directed on each switch (SW) in which the path of a I / O data was prepared by the switch in a board based on the signal from the address control section in a board (not shown).
[0026] As mentioned above, data width of face becomes possible [carrying out the division activity of the port to the crossbar switch 5 in a board with a large port] by having the structure which saves two data, and the controlling mechanism which distributes data.
[0027] In addition, in the one example of this invention, crossbar switch equipment 1 was used as the address / data discrete type, with the signal decided beforehand, using the address line, reservation of a communication path, transfer initiation, transfer termination, etc. were performed, and the structure which can output and input suitable data is realized.
[0028] Drawing 2 is the block diagram showing the configuration of the crossbar switch side I/O section 6-1 of drawing 1 . In drawing, the crossbar switch side I/O section 6-1 is equipped with the crossbar switch side address control section 61-1.
[0029] It connects with two ports of a crossbar switch 5 with the address line (A) and the 128-bit data

line (D), and the crossbar switch side I/O section 6-1 is connected to the processor board 2-1 with the address line (A), a discernment bit (bit) (Sa, Sb), and the two 128-bit data lines (a, b).
[0030] The crossbar switch side address control section 61-1 inputs the address from two ports, and outputs the address and a discernment bit to the processor board 2-1. In addition, although not illustrated, other crossbar switch side I/O sections 6-2 to 6-4 have the same composition as the above-mentioned crossbar switch side I/O section 6-1.
[0031] Drawing 3 is the block diagram showing the configuration of the data division 7-1 of drawing 1 . In drawing, data division 7-1 consist of the switch 71-1 in a board, a buffer 72-1 and 73-1, a switch (SW#1-SW#3) 74-1, 75-1 and 76-1, a buffer A group 77-1, and a buffer B group 78-1. In addition, other data divisions 7-2 to 7-4 have the same composition as the above-mentioned data division 7-1.
[0032] Drawing 4 is the block diagram showing the configuration of the address control section 8-1 of drawing 1 . In drawing, the address control section 8-1 is equipped with the address control section 81-1 in a board, and the switch control section 82-1 in a board. In addition, other address control sections 8-2 to 8-4 have the same composition as the above-mentioned address control section 8-1.
[0033] Drawing 5 is the block diagram showing the configuration of the switch 71-1 in a board of drawing 3 . In drawing, the switch 71-1 in a board is equipped with switch (SW#11-SW#20) 71a-1-71j-1.
[0034] Drawing 6 is drawing showing the example of a configuration of a switch. Drawing 6 (a) shows the configuration of switch (SW#11-SW#16) 71a-1-71f-1 shown in the switch (SW#2, SW#3) 75-1 shown in drawing 3 , 76-1, and drawing 5 . Drawing 6 (b) shows the configuration of switch (SW#17-SW#20) 71g-1-71j-1 shown in the switch (SW#1) 74-1 shown in drawing 3 , and drawing 5 .
[0035] Drawing 7 is the block diagram showing the configuration of the crossbar switch side address control section 61-1 shown in drawing 2 . The crossbar switch side address control section 61-1 consists of controller 61a-1, (Memory A) 61b-1, and (Memory B) 61c-1.
[0036] Drawing 8 (a) is drawing showing the content of storage of (Memory A) 61b-1 of drawing 7 , and drawing 8 (b) is drawing showing the content of storage of (Memory B) 61c-1 of drawing 7 . In these drawings, the board name (processor #1, processor #2, memory #1, memory #2, I/O#1, I/O#2, I/O#3, I/O#4) and the port name (a, b) are matched and memorized to (Memory A) 61b-1.
[0037] Moreover, to (Memory B) 61c-1, the communications-partner point board name of b port and the communications-partner point port name of b port were matched, respectively, and the communications-partner point board name of a port and the communications-partner point port name of a port are memorized again.
[0038] Drawing 9 is the block diagram showing the configuration of the address control section 81-1 in a board of drawing 4 . In drawing, the address control section 81-1 in a board consists of controller 81a-1, (Memory C) 81b-1, (Memory D) 81c-1, and counter 81d-1-81g-1.
[0039] Drawing 10 (a) is drawing showing the content of storage of (Memory C) 81b-1 of drawing 9 , and drawing 10 (b) is drawing showing the content of storage of (Memory D) 81c-1 of drawing 9 . In these drawings, the value of the current discernment bit Sa and the value of the current discernment bit Sb, and the value of the discernment bit Sa in front of 1 clock and the value of the discernment bit Sb in front of 1 clock are memorized by (Memory C) 81b-1.
[0040] Moreover, the address information for buffer A group 77-1 and the order information of data forwarding, and the address information and the order information of data forwarding for buffer B group 78-1 are memorized by (Memory D) 81c-1.
[0041] Here, address information AA1, AA2, AA3, and AA4 and .... show the content of an address-line signal sent in relation to the data included in the buffer A group 77-1, and the order information NAA1, NAA2, NAA3, and NAA4 of data forwarding and .. show how many the data sent to the content of a corresponding address-line signal and coincidence have been sent as data of an eye from a block head.
[0042] Address information AB1, AB2, AB3, and AB4 and .... show the content of an address-line signal sent in relation to the data included in the buffer B group 78-1, and the order information NAB1, NAB2, NAB3, and NAB4 of data forwarding and .. show how many the data sent to the content of a corresponding address-line signal and coincidence have been sent as data of an eye from a block head.

[0043] Drawing 11 is drawing showing the switch (SW#1-SW#3) 74-1 to 76-1 of drawing 3 by the switch control section 82-1 in a board of drawing 4 , and control of drawing 5 of switch (SW#11-SW#20) 71a-1-71j-1.
[0044] When connecting with Port c from the port a of the switch 71-1 in a board shown in drawing 3 and drawing 5 (a->c), and when connecting with Port d from Port b (b->d), the switch control section 82-1 in a board It controls so that switch (SW#11) 71a-1, switch (SW#13) 71c-1, switch (SW#16) 71f-1, and switch (SW#18) 71h-1 are connected to the "0" sides. It controls so that switch (SW#12) 71b-1 and switch (SW#17) 71g-1 are connected to the "1" side.
[0045] At this time, a switch (SW#1-SW#3) 74-1 to 76-1, switch (SW#14) 71d-1, switch (SW#15) 71e-1, switch (SW#19) 71i-1, and switch (SW#20) 71j-1 may be connected to any by the side of "1" a side and "0", respectively. In drawing 11 , "-" shows this condition.
[0046] When connecting with Port e from the port a of the switch 71-1 in a board (a->e), and when connecting with Port f from Port b (b->f), the switch control section 82-1 in a board It controls so that a switch (SW#2) 75-1, a switch (SW#3) 76-1, switch (SW#11) 71a-1, and switch (SW#20) 71j-1 are connected to the "0" sides. It controls so that switch (SW#12) 71b-1, switch (SW#13) 71c-1, switch (SW#16) 71f-1, and switch (SW#19) 71i-1 are connected to the "1" side.
[0047] At this time, a switch (SW#1) 74-1, switch (SW#14) 71d-1, switch (SW#15) 71e-1, switch (SW#17) 71g-1, and switch (SW#18) 71h-1 may be connected to any by the side of "1" a side and "0", respectively.
[0048] When connecting with Ports c and d from the port a of the switch 71-1 in a board (a->c, d), the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "0" sides. The switch control section 82-1 in a board synchronizes with the clock of a crossbar switch 5. Switch (SW#11) 71a-1 moreover, to the "1" "0" side a side Switch (SW#13) 71c-1 to "1", and "0" either [of near] and "0" side Switch (SW#14) 71d-1 to "0" sides or "1" side and "0" side Switch (SW#17) 71g-1 controls so that switch (SW#18) 71h-1 is connected to "1", and "0" either [of near] and "1" side alternately with a repeat at "1" side or "1" side and "0" side, respectively.
[0049] At this time, a switch (SW#1) 74-1, switch (SW#12) 71b-1, switch (SW#15) 71e-1, switch (SW#16) 71f-1, switch (SW#19) 71i-1, and switch (SW#20) 71j-1 may be connected to any by the side of "1" a side and "0", respectively.
[0050] When connecting with Ports e and f from the port a of the switch 71-1 in a board (a->e, f), the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "0" sides. The switch control section 82-1 in a board synchronizes with the clock of a crossbar switch 5. Switch (SW#11) 71a-1 moreover, to the "1" "0" side a side Switch (SW#13) 71c-1 to "1", and "0" either [of near] and "1" side Switch (SW#14) 71d-1 to "1" side or "1" side and "0" side Switch (SW#19) 71i-1 controls so that switch (SW#20) 71j-1 is connected to "1", and "0" either [of near] and "1" side alternately with a repeat at "1" side or "1" side and "0" side, respectively.
[0051] At this time, a switch (SW#1) 74-1, switch (SW#12) 71b-1, and switch (SW#15-SW#18) 71e-1-71h-1 may be connected to any by the side of "1" a side and "0", respectively.
[0052] When connecting with Ports c and d from the port b of the switch 71-1 in a board (b->c, d), the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "0" sides. The switch control section 82-1 in a board synchronizes with the clock of a crossbar switch 5. Switch (SW#12) 71b-1 moreover, to the "1" "0" side a side Switch (SW#15, SW#17) 71e-1 and 71g-1 to "1", and "0" either [of near] and "0" side It controls so that switch (SW#16, SW#18) 71f-1 and 71h-1 are connected to "0" sides or "1" side and "0" side alternately with a repeat, respectively.
[0053] At this time, a switch (SW#1) 74-1, switch (SW#11) 71a-1, switch (SW#13) 71c-1, switch (SW#14) 71d-1, switch (SW#19) 71i-1, and switch (SW#20) 71j-1 may be connected to any by the side of "1" a side and "0", respectively.
[0054] When connecting with Ports e and f from the port b of the switch 71-1 in a board (b->e, f), the

switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "0" sides. The switch control section 82-1 in a board synchronizes with the clock of a crossbar switch 5. Switch (SW#12) 71b-1 moreover, to the "1" "0" side a side Switch (SW#15) 71e-1 to "1", and "0" either [of near] and "1" side Switch (SW#16) 71f-1 to "1" side or "1" side and "0" side Switch (SW#19) 71i-1 controls so that switch (SW#20) 71j-1 is connected to "1", and "0" either [of near] and "0" side alternately with a repeat at "0" sides or "1" side and "0" side, respectively.

[0055] At this time, a switch (SW#1) 74-1, switch (SW#11) 71a-1, switch (SW#13) 71c-1, switch (SW#14) 71d-1, switch (SW#17) 71g-1, and switch (SW#18) 71h-1 may be connected to any by the side of "1" a side and "0", respectively.

[0056] When connecting with Port a from the ports c and d of the switch 71-1 in a board (c, d->a), the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "1" side. The switch control section 82-1 in a board synchronizes with the clock of a crossbar switch 5. Switch (SW#11) 71a-1 moreover, to the "0" "1" side a side Switch (SW#13) 71c-1 to "0" sides or "1" side and "0" side Switch (SW#14) 71d-1 to "1", and "0" either [of near] and "0" side Switch (SW#17) 71g-1 controls so that switch (SW#18) 71h-1 is connected to "1" side or "1" side and "0" side alternately with a repeat at "1", and "0" either [of near] and "1" side, respectively.

[0057] At this time, a switch (SW#1) 74-1, switch (SW#12) 71b-1, switch (SW#15) 71e-1, switch (SW#16) 71f-1, switch (SW#19) 71i-1, and switch (SW#20) 71j-1 may be connected to any by the side of "1" a side and "0", respectively.

[0058] When connecting with Port b from the ports c and d of the switch 71-1 in a board (c, d->b), the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "1" side. The switch control section 82-1 in a board synchronizes with the clock of a crossbar switch 5. Switch (SW#12) 71b-1 moreover, to the "0" "1" side a side Switch (SW#15) 71e-1 to "0" sides or "1" side and "0" side Switch (SW#16) 71f-1 to "1", and "0" either [of near] and "0" side Switch (SW#19) 71i-1 controls so that switch (SW#20) 71j-1 is connected to "0" sides or "1" side and "0" side alternately with a repeat at "1", and "0" either [of near] and "0" side, respectively.

[0059] At this time, a switch (SW#1) 74-1, switch (SW#11) 71a-1, switch (SW#13) 71c-1, switch (SW#14) 71d-1, switch (SW#17) 71g-1, and switch (SW#18) 71h-1 may be connected to any by the side of "1" a side and "0", respectively.

[0060] When connecting with the output side of the switch 71-1 in a board, the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "0" sides.

[0061] At this time, a switch (SW#1) 74-1 and switch (SW#11-SW#20) 71a-1-71j-1 may be connected to any by the side of "1" a side and "0", respectively.

[0062] When connecting with the input side of the switch 71-1 in a board, the switch control section 82-1 in a board is controlled so that a switch (SW#2) 75-1 and a switch (SW#3) 76-1 are connected to the "1" side.

[0063] At this time, a switch (SW#1) 74-1 and switch (SW#11-SW#20) 71a-1-71j-1 may be connected to any by the side of "1" a side and "0", respectively.

[0064] When the switch 71-1 in a board is connected to the output of the buffer A group 77-1, the switch control section 82-1 in a board is controlled so that a switch (SW#1) 74-1 is connected to the "1" side.

[0065] At this time, a switch (SW#2, SW#3) 75-1, 76-1, and switch (SW#11-SW#20) 71a-1-71j-1 may be connected to any by the side of "1" a side and "0", respectively.

[0066] When the switch 71-1 in a board is connected to the output of the buffer B group 78-1, the switch control section 82-1 in a board is controlled so that a switch (SW#1) 74-1 is connected to the "0" sides.

[0067] At this time, a switch (SW#2, SW#3) 75-1, 76-1, and switch (SW#11-SW#20) 71a-1-71j-1 may be connected to any by the side of "1" a side and "0", respectively.

[0068] With reference to these drawing 1 - drawing 11 , the crossbar switch equipment 1 by one

example of this invention is explained. It connects with each port of a crossbar switch 5, and the I/O board (#1-#4) 4-1 to 4-4 is using only a part for one port of a crossbar switch 5.
[0069] On the other hand, it connects with each port of a crossbar switch 5 through the crossbar switch side I/O section 6-1 to 6-4 shown in drawing 2 , and the processor board 2-1, 2-2 and the memory board 3-1, and 3-2 are using a part for two ports of a crossbar switch 5.
[0070] The crossbar switch side I/O section 6-1 to 6-4 is connected to the data division 7-1 to 7-4 and the address control section 8-1 to 8-4 in each board shown in drawing 3 and drawing 4 . In the crossbar switch side I/O section 6-1 to 6-4, after are vacant with a discernment bit and checking a port to the transfer request via the conventional crossbar switch, the propriety of a transfer is answered, or a transfer request is performed to the crossbar switch side address control section 61-1 to which the suitable board was connected in response to the transfer request from the connected board.
[0071] The data division 7-1 to 7-4 in each board shown in drawing 3 consist of the switch 74-1 for data distribution, 75-1, 76-1, two buffer A groups 77-1, and a buffer B group 78-1. The address control section 8-1 to 8-4 in each board shown in drawing 4 consists of an address control section 81-1 in a board, and a switch control section 82-1 in a board.
[0072] from two or more interconnect of switch 71a-1-71j-1 which shows the switch 71-1 in a board of data division 7-1 to 7-4 to drawing 5 -- becoming -- the directions from the switch control section 82-1 in a board -- being based -- each -- switch 71a-1-71j-1 is changed. Without gathering the input data to each board for every port, and the conventional board being conscious of data width of face, the buffer A group 77-1 and the buffer B group 78-1 hold data by 256-bit width of face so that data can be received.
[0073] The address control section 81-1 in a board of the address control section 8-1 to 8-4 As shown in drawing 9 , the address line and the discernment bit line (Sa, Sb) to a crossbar switch 5, Conventionally which are indicated to be a and b port discernment line to drawing 40 The signal line to the controller 22-1 of equipment, The signal line for data incorporation timing to the buffer A group 77-1 and the buffer B group 78-1, It connects with the 128-bit buffer 72-1 of the preceding paragraph, and the signal line for data incorporation timing of 73-1 conventionally at the signal line for data incorporation timing to the input buffer 23-1 of equipment, respectively.
[0074] The address control section 81-1 in a board updates a discernment bit in response to the transfer request from the controller 22-1 of equipment conventionally, and performs a transfer request to a crossbar switch 5 side. Moreover, the address control section 81-1 in a board recognizes the width of face and the port of data which are transmitted from the information on a discernment bit in response to the transfer request from a crossbar switch 5 side, incorporates data to the buffer A group 77-1 and the buffer B group 78-1, and transmits the data to the timing of the opening of the data I/O section of equipment conventionally.
[0075] The switch control section 82-1 in a board will direct by changing to a required switch with reference to the content shown in drawing 11 , if the directions from the address control section 81-1 in a board are received.
[0076] If drawing 7 is referred to, the configuration of the address control section 61-1 in the crossbar switch side I/O section 6-1 shown in drawing 2 is shown, and the address control section 61-1 consists of controller 61a-1, (Memory A) 61b-1, and (Memory B) 61c-1.
[0077] (Memory A) 61b-1 becomes a means for getting to know whether the configuration environment of the crossbar switch equipment 1 whole is memorized, and [referring to drawing 8 (a)] and the corresponding communications partner have the possibility of a 256-bit width-of-face transfer. In case (Memory B) 61c-1 memorizes a partner's board name and port name under communication link now and it transmits the signal of [refer to drawing 8 (b)] and the address line, it is referred to.
[0078] If drawing 9 is referred to, the detailed configuration of the address control section 81-1 in a board shown in drawing 4 is shown, and the address control section 81-1 in a board consists of controller 81a-1, (Memory C) 81b-1, (Memory D) 81c-1, and counter 81d-1-81g-1.
[0079] (Memory C) 81b-1 becomes a means for controller 81a-1 to get to know that from which the value in front of 1 clock of the discernment bits Sa and Sb was held, and the value changed with [refer to

drawing 10 (a)] and an applicable clock.
[0080] (Memory D) 81c-1 the contents AA1, AA2, AA3, and AA4 of an address signal sent with the data of the buffer A group 77-1 of data division 7-1, and the buffer B group 78-1, ..., AB1, AB2, AB3 and AB4, and .. simultaneous -- sending -- having had -- data -- specifying -- record -- NAA -- one -- NAA -- two -- NAA -- three -- NAA -- four .... NAB -- one -- NAB -- two -- NAB -- three -- NAB -- four .. holding -- [-- drawing 10 -- (-- b --) -- reference --] .
[0081] Counter 81d-1-81g-1 shows the data of which offer the data of what position of a block in the data input section of equipment conventionally with whether close is, respectively to the buffer A group 77-1 and the buffer B group 78-1.
[0082] When sending the clock for data incorporation to the buffer A group 77-1 and the buffer B group 78-1, this Count-up directions are outputted to counter 81d-1 which corresponds simultaneously, and 81f-1. When sending data incorporation directions to the buffer of the data input section of equipment conventionally Simultaneously, output count-down directions to counter 81d-1 and 81f-1, and count-up directions are outputted to counter 81e-1 and 81g-1, respectively. It realizes by sending zero reset directions to counter 81e-1 and 81g-1 conventionally with data incorporation directions of the last of the block data to the buffer of the data input section of equipment.
[0083] Drawing 12 - drawing 15 are flow charts which show the actuation of the crossbar switch side address control section 61-1 shown in drawing 2 and drawing 7 , and drawing 16 - drawing 23 are flow charts which show the actuation of the address control section 81-1 in a board shown in drawing 4 and drawing 9 .
[0084] With reference to these drawing 1 - drawing 23 , actuation of the crossbar switch equipment 1 by one example of this invention is explained. In addition, performing the program of the control memory which each control section does not illustrate can also be realized, and actuation of the above-mentioned flow chart has usable ROM (read-only memory) etc. as a control memory.
[0085] Drawing 12 - drawing 15 show actuation in case the processor board 2-1 by which direct continuation was carried out to the crossbar switch side address control section 61-1 performs a transfer request. In this case, the crossbar switch side address control section 61-1 will check the empty situation of the port of a self-circuit with reference to a discernment bit, if the processor board 2-1 connected is a 256-bit board when a transfer request is received through the address line from the address control section 81-1 in a board of the address control section 8-1 of the processor board 2-1 (drawing 12 step S1) (drawing 12 step S2) (drawing 12 step S3).
[0086] If 256 bits of ports of a crossbar switch 5 are securable (drawing 12 step S4) (i.e., if two ports of the crossbar switch 5 to which the crossbar switch side I/O section 6-1 is connected are securable), the crossbar switch side address control section 61-1 will check the maximum data width of face of a communications partner with reference to (Memory A) 61b-1 (drawing 12 step S5).
[0087] The crossbar switch side address control section 61-1 will send a transfer request to the two address lines corresponding to the ports a and b of a communications partner, if the maximum data width of face of the communications partner is 256-bit width of face (drawing 12 step S6) (drawing 12 step S7), and if it is 128 bits, it will send a transfer request to the address line (1) corresponding to the port of a communications partner (drawing 12 step S12).
[0088] The crossbar switch side address control section 61-1 will relay the signal to the address control section 81-1 in a board of the processor board 2-1, if Transfer O.K. comes on the contrary from both two address lines (drawing 12 step S8). The crossbar switch side address control section 61-1 relays a signal in the path same till transfer termination henceforth (drawing 12 step S9).
[0089] On the other hand, the crossbar switch side address control section 61-1 changes the discernment bit corresponding to one of ports into "0" by the approach decided beforehand, when there is transfer O.K. only from the one address line (drawing 14 step S18) (drawing 14 step S19).
[0090] A discernment bit secures the near path of "1" and the crossbar switch side address control section 61-1 relays a transfer O.K. signal to the address control section 81-1 in a board of the processor board 2-1 (drawing 14 step S20).
[0091] In this case, the crossbar switch side address control section 61-1 records the path and phase hand

information which were secured to (Memory B) 61c-1 (drawing 14 step S20). Henceforth, with reference to the path and phase hand information which were recorded on (Memory B) 61c-1, it checks about the signal from the address control section 81-1 in a board, and if it is a signal from the same communications partner, the junction of the signal will be continued till transfer termination (drawing 14 step S21). In addition, if the crossbar switch side address control section 61-1 becomes transfer termination, it will eliminate the path information on (Memory B) 61c-1 simultaneously (drawing 14 step S22).

[0092] The crossbar switch side address control section 61-1 relays the signal to the address control section 81-1 in a board of the processor board 2-1, when a transfer failure comes on the contrary from both address lines (drawing 14 step S23) (drawing 14 step S24).

[0093] On the other hand, if the port of the processor board 2-1 can secure only 128-bit width of face (drawing 12 step S10), the crossbar switch side address control section 61-1 is chosen by the approach which was able to determine the one address line of a partner beforehand, and sends a transfer request (drawing 12 step S11).

[0094] If Transfer O.K. comes on the contrary to the transfer request (drawing 14 step S18), the crossbar switch side address control section 61-1 will secure a path like the above (drawing 14 step S20), and will relay Transfer O.K. to the address control section 81-1 in a board of the processor board 2-1 (drawing 14 step S21).

[0095] Also in this case, the crossbar switch side address control section 61-1 records the path and phase hand information which were secured to (Memory B) 61c-1 (drawing 14 step S20). Henceforth, with reference to the path and phase hand information which were recorded on (Memory B) 61c-1, it checks about the signal from the address control section 81-1 in a board, and if it is a signal from the same communications partner, the junction of the signal will be continued till transfer termination (drawing 14 step S21). In addition, if the crossbar switch side address control section 61-1 becomes transfer termination, it will eliminate the path information on (Memory B) 61c-1 simultaneously (drawing 14 step S22).

[0096] The crossbar switch side address control section 61-1 relays the signal to the same address control section 81-1 in a board, also when a transfer failure comes on the contrary (drawing 14 step S23) (drawing 14 step S24).

[0097] When the port of the processor board 2-1 is not 256 bits (drawing 12 step S2), the crossbar switch side address control section 61-1 relays the signal of a transfer request to the address line according to the data width of face of a communications partner with reference to (Memory A) 61b-1 (drawing 13 step S13).

[0098] The crossbar switch side address control section 61-1 will relay Transfer O.K. to the address control section 81-1 in a board of the processor board 2-1 like the above, if Transfer O.K. comes on the contrary to the transfer request (drawing 13 step S14). Henceforth, the crossbar switch side address control section 61-1 continues the junction of the signal till transfer termination (drawing 13 step S15).

[0099] The crossbar switch side address control section 61-1 relays the signal to the same address control section 81-1 in a board, also when a transfer failure comes on the contrary (drawing 13 step S16) (drawing 13 step S17).

[0100] As for drawing 15 , the crossbar switch side address control section 61-1 shows actuation of a carrier beam case for the transfer request from the crossbar switch 5 side. In this case, the crossbar switch side address control section 61-1 will check the empty situation of the port of a self-circuit with reference to a discernment bit, if a transfer request is received from a crossbar switch 5 side (drawing 15 step S31) (drawing 15 step S32).

[0101] If the processor board 2-1 to which the crossbar switch side address control section 61-1 is connected is a 256-bit board (drawing 15 step S33), a transfer request will judge whether it came from the two address lines (drawing 15 step S34).

[0102] It investigates whether the crossbar switch side address control section 61-1 can secure the port of a transfer request, if the transfer request is coming from the two address lines (drawing 15 step S35). If reservation of the port of a transfer request is possible for the crossbar switch side address control

section 61-1, by both changing the discernment bits Sa and Sb into "1", it will secure (drawing 15 step S36), and Transfer O.K. will be returned through the address line corresponding to the secured discernment bit (drawing 15 step S37).
[0103] The crossbar switch side address control section 61-1 transmits a transfer request to the address control section 81-1 in a board (drawing 15 step S38), a transfer path and partner information are memorized to (Memory B) 61c-1, and henceforth, with reference to the content of (Memory B) 61c-1, if the signal from the applicable address line is a signal from an applicable port, it will relay this to the address control section 81-1 in a board (drawing 15 step S39).
[0104] At this time, the address control section 81-1 in a board is an address signal from the data transfer point of a port, when 1-bit a and b port discernment line are "0", and it identifies that it is an address signal from the data transfer point of b port at the time of "1."
[0105] The crossbar switch side address control section 61-1 clears the content of (Memory B) 61c-1 after transfer termination, and the discernment bit changed into "1" is returned (drawing 15 step S40).
[0106] If the processor board 2-1 connected is vacant as for (the drawing 15 step S33) and a corresponding port on the 128-bit board (drawing 15 step S41), the crossbar switch side address control section 61-1 will relay a transfer request as it is, and will relay and return the answerback to the empty situation of equipment conventionally (drawing 15 step S42). Henceforth, the crossbar switch side address control section 61-1 performs the same actuation as the above (drawing 15 steps S38-S40).
[0107] If the corresponding port is not vacant (drawing 15 step S41), if the port is not vacant while the transfer request is not coming from the two address lines (drawing 15 steps S34 and S43), or if the crossbar switch side address control section 61-1 cannot secure the port of a transfer request (drawing 15 step S44), it returns a transfer failure in a path with a transfer request (drawing 15 step S47).
[0108] One crossbar switch side address control section 61-1 will change the discernment bit corresponding to an empty port into "1", if the port of a transfer request can be secured when a transfer request does not come from the two address lines (drawing 15 step S43), or if the port of a transfer request can secure while the transfer request is coming from the two address lines (drawing 15 step S44) (drawing 15 step S45).
[0109] The crossbar switch side address control section 61-1 returns Transfer O.K. using the address line corresponding to the secured port (drawing 15 step S46), and performs the same actuation as the above henceforth (drawing 15 steps S38-S40).
[0110] Actuation of the address control section 81-1 (not mounted in the 128-bit board) in a board of the address controller section 8-1 of processor board 2- is shown in drawing 16 - drawing 23 . In this case, if a transfer request is received from the controller 22-1 (refer to drawing 40) of equipment conventionally by which direct continuation was carried out (drawing 16 step S51), the address control section 81-1 in a board will check that the ports c and d of the switch 71-1 in a board of the data division 7-1 of the processor board 2-1 are not used, and will relay a transfer request as it is (drawing 16 step S52). When used, a transfer failure is returned to a controller 22-1.
[0111] Then, if the address control section 81-1 in a board receives the advice of transfer O.K. from the destination, and checks a discernment bit (drawing 17 steps S61 and S62) and a 256-bit band can be secured If it is Sa=1 and Sb=1 (drawing 17 step S63), to the switch control section 82-1 in a board so that data can be directly sent out to this namely, a path That is, reservation of c->a and a d->b path and modification for a switch (SW#2, #3) 75-1 and the sending-area path of 76-1 are directed (drawing 17 step S64).
[0112] Then, the address control section 81-1 in a board transmits the clock of a crossbar switch 5 to the output buffer 24-1 (refer to drawing 40) of equipment conventionally, and enables sending out of a ** clock and new data on a crossbar switch 5 (drawing 17 step S65).
[0113] The address control section 81-1 in a board relays the address-line signal from a controller 22-1 as it is till the completion of a transfer (drawing 17 step S66), and returns the discernment bits Sa and Sb to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (drawing 17 step S67).
[0114] The address control section 81-1 in a board will direct to operate in the mode which changes a

path to the switch control section 82-1 in a board for every clock so that data can be sent in an order from c and d, if only 128 bits of bands are securable (drawing 17 step S68) (i.e., if discernment bits are Sa=1 and Sb=0), or if discernment bits are Sa=0 and Sb=1 (drawing 18 step S74).
[0115] When discernment bits are Sa=1 and Sb=0, the address control section 81-1 in a board directs reservation of a c->a path, and modification to a switch (SW#2, #3) 75-1 and the sending area of 76-1 to the switch control section 82-1 in a board (drawing 17 step S69).
[0116] Henceforth, it is directed to the switch control section 82-1 in a board that the address control section 81-1 in a board changes the path of c->a, and the path of d->a for every clock of a crossbar switch 5 (drawing 17 step S70). The address control section 81-1 in a board transmits the clock of a crossbar switch 5 to the output buffer 24-1 of equipment once conventionally at 2 times, and enables sending out of data new once on a crossbar switch 5 at two clocks (drawing 17 step S71).
[0117] The address control section 81-1 in a board relays the address-line signal from a controller 22-1 as it is till the completion of a transfer (drawing 17 step S72), and returns the discernment bit Sa to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (drawing 17 step S73).
[0118] When discernment bits are Sa=0 and Sb=1, the address control section 81-1 in a board directs reservation of a c->b path, and modification to a switch (SW#2, #3) 75-1 and the sending area of 76-1 to the switch control section 82-1 in a board (drawing 18 step S75).
[0119] Henceforth, it is directed to the switch control section 82-1 in a board that the address control section 81-1 in a board changes the path of c->b, and the path of d->b for every clock of a crossbar switch 5 (drawing 18 step S76). The address control section 81-1 in a board transmits the clock of a crossbar switch 5 to the output buffer 24-1 of equipment once conventionally at 2 times, and enables sending out of data new once on a crossbar switch 5 at two clocks (drawing 18 step S77).
[0120] The switch control section 82-1 in a board relays the address-line signal from a controller 22-1 as it is till the completion of a transfer (drawing 18 step S78), and returns the discernment bit Sb to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (drawing 18 step S79).
[0121] If the address control section 81-1 in a board cannot secure the above-mentioned band, it relays a transfer failure to the controller 22-1 of equipment conventionally, and leaves resending etc. to equipment conventionally (drawing 18 step S80).
[0122] As for drawing 19 - drawing 23 , the address control section 81-1 in a board shows actuation of a carrier beam case for the transfer request from the controller 22-1 of equipment conventionally via the crossbar switch 5. In this case, the address control section 81-1 in a board investigates the discernment bit which changed to "1" compared with 1 clock front with reference to (Memory C) 81b-1 (drawing 19 steps S91 and S92), and recognizes the port to which data are sent.
[0123] The address control section 81-1 in a board chooses the usable buffer A group 77-1 or the buffer B group 78-1 which becomes clear from this information and the check of a path in use, and directs a suitable path to the switch control section 82-1 in a board.
[0124] At this time, when 128 bits of data are sent at a time, it is sending a clock to the buffer 72-1, 73-1 and the buffer A group 77-1, or the buffer B group 78-1 of the preceding paragraph by turns, and step is kept with 256-bit data and it memorizes in the buffer A group 77-1 or the buffer B group 78-1.
[0125] In parallel to this, on the other hand, in order that the address control section 81-1 in a board may make the controller 22-1 by which direct continuation is carried out receive data, a transfer request is sent out. A transfer request is repeated when a controller 22-1 cannot receive data for data from another buffer group because of the transfer middle class.
[0126] When Transfer O.K. comes on the contrary, the address control section 81-1 in a board makes a switch (SW#1) 74-1 changed to an applicable buffer side, starts the clock sending to the input buffer 23-1 (refer to drawing 40) of equipment conventionally simultaneously, and makes the data in a buffer incorporate. However, this clock is sent only when 256-bit data exist in an applicable buffer, referring to counter 81d-1-81g-1.
[0127] The actuation which sends a control signal is shown in a buffer below from the address control

section 81-1 in a board when storing data in the buffer of data division 7-1. When data are transmitted by the transfer partner and 256-bit width of face, the address control section 81-1 in a board sends a data incorporation signal to the 128-bit buffer of an applicable buffer group and the preceding paragraph synchronizing with the clock by the side of a crossbar switch 5. Simultaneously, the direction where counter 81d-1 of the address control section 81-1 in a board or counter 81e-1 correspond either is counted up.

[0128] Similarly, when having received data by 128 bits, the address control section 81-1 in a board is incorporated to the preceding paragraph buffer which corresponds to the timing of 128 bits of low order received first. Directions Delivery, While sending a signal to an applicable buffer group to the following clock timing by the side of a crossbar switch 5 and depressing old data In accordance with 128 bits of high orders which are directly visible through the switch 71-1 in a board, and the data for 128 bits of low order which a preceding paragraph buffer has, it incorporates as new data. Simultaneously, the direction where counter 81d-1 of the address control section 81-1 in a board or counter 81e-1 correspond is counted up.

[0129] Conventionally by which direct continuation was carried out from the buffer of data division 7-1, data transfer to the data input section of equipment is performed, after the address control section 81-1 in a board by which direct continuation was carried out receives the signal of the transfer O.K. from the controller 22-1 to an applicable data block.

[0130] With reference to counter 81d-1-81g-1, this data transfer sends conventionally the usual clock signal defined beforehand to the clock line of the buffer of the data input section of equipment, when 256-bit data are stored in the buffer group. When there are no 256-bit data in the buffer group, transfer of a clock signal is shelved.

[0131] Namely, when the address control section 81-1 in a board has transmitted data by the transfer partner and 256-bit width of face, That is, when the discernment bit is changing with Sa=0 ->1 and Sb=0 ->1 (drawing 19 step S93), Reservation of a->c and a b->d path and modification for a switch (SW#2, #3) 75-1 and the sending-area path of 76-1 are directed to the switch control section 82-1 in a board (drawing 19 step S94).

[0132] The address control section 81-1 in a board will direct to change a switch (SW#1) 74-1 to the buffer A group 77-1 to the switch control section 82-1 in a board, if the transfer request to the controller 22-1 of equipment is O.K. conventionally (drawing 19 step S95) (drawing 19 step S96). The address control section 81-1 in a board will accumulate the transfer request of the address line in the buffer for the addresses for buffer A group 77-1 of (Memory D) 81c-1, if the transfer request to the controller 22-1 of equipment is NG conventionally (drawing 19 step S95) (drawing 19 step S99).

[0133] The address control section 81-1 in a board relays address information AAn to corresponding data and coincidence conventionally at the controller 22-1 of equipment with reference to Record NAAn (n= 1, 2, 3 and 4, ...) and the clock signal of (Memory D) 81c-1, and transmits the clock of a crossbar switch 5 of operation to the input buffer 23-1 of each time and conventional equipment as it is (drawing 19 step S97). The address control section 81-1 in a board returns the discernment bits Sa and Sb to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (drawing 19 step S98).

[0134] Moreover, the address control section 81-1 in a board checks the connection path of Port b, when data are transmitted by the transfer partner and 128-bit width of face (drawing 20 step S100) (i.e., when the discernment bit is changing with Sa=0 ->1) (drawing 20 step S101).

[0135] The address control section 81-1 in a board will direct to change into reservation of a->e and f path to the switch control section 82-1 in a board, if Port b is connected to the buffer A group 77-1 (drawing 20 step S102) (drawing 20 step S103).

[0136] The address control section 81-1 in a board will direct to change a switch (SW#1) 74-1 to the buffer B group 78-1 to the switch control section 82-1 in a board, if the transfer request to the controller 22-1 of equipment is O.K. conventionally (drawing 20 step S104) (drawing 20 step S105). The address control section 81-1 in a board will accumulate the transfer request of the address line in the buffer for the addresses for buffer B group 78-1 of (Memory D) 81c-1, if the transfer request to the controller 22-1

of equipment is NG conventionally (drawing 20 step S104) (drawing 20 step S109).
[0137] If the address control section 81-1 in a board has data of 256-bit width of face in the buffer B group 78-1 (drawing 20 step S106) Record NABn (n= 1, 2, 3 and 4, ...) and the clock signal of (Memory D) 81c-1 are referred to. Address information ABn is conventionally relayed to corresponding data and coincidence at the controller 22-1 of equipment, and the clock of a crossbar switch 5 of operation is transmitted to the input buffer 23-1 of each time and conventional equipment as it is (drawing 20 step S107). The address control section 81-1 in a board returns the discernment bit Sa to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (drawing 20 step S108).
[0138] The address control section 81-1 in a board directs reservation of a->c and d path, and modification for a switch (SW#2, #3) 75-1 and the sending-area path of 76-1 to the switch control section 82-1 in a board, if Port b is not connected to the buffer A group 77-1 (drawing 20 step S102) (drawing 22 step S119).
[0139] The address control section 81-1 in a board will direct to change a switch (SW#1) 74-1 to the buffer A group 77-1 to the switch control section 82-1 in a board, if the transfer request to the controller 22-1 of equipment is O.K. conventionally (drawing 22 step S120) (drawing 22 step S121). The address control section 81-1 in a board will accumulate the transfer request of the address line in the buffer for the addresses for buffer A group 77-1 of (Memory D) 81c-1, if the transfer request to the controller 22-1 of equipment is NG conventionally (drawing 22 step S120) (drawing 22 step S125).
[0140] If the address control section 81-1 in a board has data of 256-bit width of face in the buffer A group 77-1 (drawing 22 step S122) Record NAAn (n= 1, 2, 3 and 4, ...) and the clock signal of (Memory D) 81c-1 are referred to. Address information AAn is conventionally relayed to corresponding data and coincidence at the controller 22-1 of equipment, and the clock of a crossbar switch 5 of operation is transmitted to the input buffer 23-1 of each time and conventional equipment as it is (drawing 22 step S123). The address control section 81-1 in a board returns the discernment bit Sa to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (drawing 22 step S124).
[0141] The address control section 81-1 in a board will direct to change into reservation of a->e and f path to the switch control section 82-1 in a board, if Port a is connected to the buffer A group 77-1 when data are transmitted by the transfer partner and 128-bit width of face (drawing 21 step S110) (i.e., when the discernment bit is changing with Sb=0 ->1) (drawing 21 step S111) (drawing 21 step S112).
[0142] The address control section 81-1 in a board will direct to change a switch (SW#1) 74-1 to the buffer B group 78-1 to the switch control section 82-1 in a board, if the transfer request to the controller 22-1 of equipment is O.K. conventionally (drawing 21 step S113) (drawing 21 step S114). The address control section 81-1 in a board will accumulate the transfer request of the address line in the buffer for the addresses for buffer B group 78-1 of (Memory D) 81c-1, if the transfer request to the controller 22-1 of equipment is NG conventionally (drawing 21 step S113) (drawing 21 step S118).
[0143] If the address control section 81-1 in a board has data of 256-bit width of face in the buffer B group 78-1 (drawing 21 step S115) Record NABn (n= 1, 2, 3 and 4, ...) and the clock signal of (Memory D) 81c-1 are referred to. Address information ABn is conventionally relayed to corresponding data and coincidence at the controller 22-1 of equipment, and the clock of a crossbar switch 5 of operation is transmitted to the input buffer 23-1 of each time and conventional equipment as it is (drawing 21 step S116). The address control section 81-1 in a board returns the discernment bit Sb to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (drawing 21 step S117).
[0144] The address control section 81-1 in a board directs reservation of a->c and d path, and modification for a switch (SW#2, #3) 75-1 and the sending-area path of 76-1 to the switch control section 82-1 in a board, if Port a is not connected to the buffer A group 77-1 (drawing 21 step S111) (drawing 23 step S126).
[0145] The address control section 81-1 in a board will direct to change a switch (SW#1) 74-1 to the buffer A group 77-1 to the switch control section 82-1 in a board, if the transfer request to the controller

22-1 of equipment is O.K. conventionally (drawing 23 step S127) (drawing 23 step S128). The address control section 81-1 in a board will accumulate the transfer request of the address line in the buffer for the addresses for buffer A group 77-1 of (Memory D) 81c-1, if the transfer request to the controller 22-1 of equipment is NG conventionally (drawing 23 step S127) (drawing 23 step S132).

[0146] If the address control section 81-1 in a board has data of 256-bit width of face in the buffer A group 77-1 (drawing 23 step S129) Record NAAn (n= 1, 2, 3 and 4, ...) and the clock signal of (Memory D) 81c-1 are referred to. Address information AAn is conventionally relayed to corresponding data and coincidence at the controller 22-1 of equipment, and the clock of a crossbar switch 5 of operation is transmitted to the input buffer 23-1 of each time and conventional equipment as it is (drawing 23 step S130). The address control section 81-1 in a board returns the discernment bit Sb to "0" taking advantage of the completion signal of a transfer having been sent from the controller 22-1 (drawing 23 step S131).

[0147] Drawing 24 is drawing in which showing a division in the case of the data transfer in the crossbar switch equipment 1 by one example of this invention. In drawing, C1 shows the case where a 256-bit band can be secured in case 256-bit data are transmitted to a 256-bit port, C2 shows the case where a 128-bit band can be secured in case 256-bit data are transmitted to a 256-bit port, and in case C3 transmits 256-bit data to a 256-bit port, it shows the case where a band is not securable.

[0148] C4 shows the case where a 128-bit band can be secured in case 128-bit data are transmitted to a 256-bit port, and in case C5 transmits 128-bit data to a 256-bit port, it shows the case where a band is not securable.

[0149] C6 shows the case where a 128-bit band can be secured in case 256-bit data are transmitted to a 128-bit port, and in case C7 transmits 256-bit data to a 128-bit port, it shows the case where a band is not securable.

[0150] C8 shows the case where a 128-bit band can be secured in case 128-bit data are transmitted to a 128-bit port, and in case C9 transmits 128-bit data to a 128-bit port, it shows the case where a band is not securable.

[0151] In case drawing 25 transmits the 256-bit data based on one example of this invention to a 256-bit port, it is drawing showing actuation of a requestor side when a 256-bit band is securable (in the case of C1), and in case drawing 26 transmits the 256-bit data based on one example of this invention to a 256-bit port, it is drawing showing the actuation by the side of supply when a 256-bit band is securable (in the case of C1).

[0152] In case drawing 27 transmits the 256-bit data based on one example of this invention to a 256-bit port, it is drawing showing actuation of a requestor side when a 128-bit band is securable (in the case of C2), and in case drawing 28 transmits the 256-bit data based on one example of this invention to a 256-bit port, it is drawing showing the actuation by the side of supply when a 128-bit band is securable (in the case of C2).

[0153] In case drawing 29 transmits the 256-bit data based on one example of this invention to a 256-bit port, it is drawing showing actuation of a requestor side when a band is not securable (in the case of C3), and in case drawing 30 transmits the 256-bit data based on one example of this invention to a 256-bit port, it is drawing showing the actuation by the side of supply when a band is not securable (in the case of C3).

[0154] In case drawing 31 transmits the 128-bit data based on one example of this invention to a 256-bit port, it is drawing showing actuation of a requestor side when a 128-bit band is securable (in the case of C4), and in case drawing 32 transmits the 128-bit data based on one example of this invention to a 256-bit port, it is drawing showing the actuation by the side of supply when a 128-bit band is securable (in the case of C4).

[0155] In case drawing 33 transmits the 128-bit data based on one example of this invention to a 256-bit port, it is drawing showing actuation of a requestor side when a band is not securable (in the case of C5), and in case drawing 34 transmits the 128-bit data based on one example of this invention to a 256-bit port, it is drawing showing the actuation by the side of supply when a band is not securable (in the case of C5).

[0156] In case drawing 35 transmits the 256-bit data based on one example of this invention to a 128-bit port, it is drawing showing actuation of a requestor side when a 128-bit band is securable (in the case of C6), and in case drawing 36 transmits the 256-bit data based on one example of this invention to a 128-bit port, it is drawing showing the actuation by the side of supply when a 128-bit band is securable (in the case of C6).
[0157] In case drawing 37 transmits the 256-bit data based on one example of this invention to a 128-bit port, it is drawing showing actuation of a requestor side when a band is not securable (in the case of C7), and in case drawing 38 transmits the 256-bit data based on one example of this invention to a 128-bit port, it is drawing showing the actuation by the side of supply when a band is not securable (in the case of C7).
[0158] With reference to these drawing 1 - drawing 11 and drawing 24 - drawing 38, the data transfer using the crossbar switch equipment 1 by one example of this invention is explained. In addition, in the case of C8 and C9 which are shown in drawing 24, it is the conventionally same environment as equipment, and since it is obvious, the actuation is not explained especially.
[0159] First, in case 256-bit data are transmitted to a 256-bit port, when a 256-bit band can be secured (in the case of C1), If there is a transfer request from the controller 22-1 of equipment conventionally when the discernment bits Sa and Sb are "0" in both requestor sides (processing C 1-1) The address control section 81-1 in a board makes the discernment bits Sa and Sb both "1", and sends out a transfer request (processing C 1-2 (Sa=0 ->1, Sb=0 ->1)). Here, in both supply sides, the discernment bits Sa and Sb are "0" at processing C-1 and the time of C-2.
[0160] Then, the crossbar switch side address control section 61-1 of a requestor side sends out a transfer request to the two address lines of a communications partner, if the discernment bits Sa and Sb become both "1." The crossbar switch side address control section 61-1 by the side of supply detects the transfer request of the two address lines. At this time, in a requestor side, the discernment bits Sa and Sb are "1" and supply sides, and are "0" (processing C 1-3).
[0161] Since the discernment bits Sa and Sb are "0", both the crossbar switch side address control sections 61-1 by the side of supply answer Transfer O.K. to both two address lines, both set the discernment bits Sa and Sb to "1" (Sa=0 ->1, Sb=0 ->1) simultaneously, and send out a transfer request to a board. Then, the address control section 81-1 in a board by the side of supply directs routing of a->c and b->d to the switch control section 82-1 in a board (processing C 1-4).
[0162] The address control section 81-1 in a board by the side of supply transmits a transfer request to the controller 22-1 of equipment conventionally. If Transfer O.K. is checked from both two address lines, the crossbar switch side address control section 61-1 of a requestor side will both consider the discernment bits Sa and Sb as as ["1"], and will transmit Transfer O.K. to a board (processing C 1-5).
[0163] The switch control section 82-1 in a board of a requestor side directs routing of a->c and b->d to the switch control section 82-1 in a board, and directs to make a switch (SW#2, SW#3) 75-1 and 76-1 into a sending area (processing C 1-6).
[0164] The switch control section 82-1 in a board of a requestor side sends out data, if directed setting out is performed. The switch control section 82-1 in a board by the side of supply receives the sent data by the buffer A group 77-1 (processing C 1-7).
[0165] The data input section of equipment incorporates the address control section 81-1 in a board by the side of supply conventionally from a buffer group, and it does not have inner data, or checks incorporation termination (processing C 1-8).
[0166] The address control section 81-1 in a board by the side of supply sends the address to the controller of equipment conventionally after a check. The crossbar switch side address control section 61-1 directs to set a switch (SW#1) 74-1 as the buffer A group 77-1 (processing C 1-9).
[0167] The address control section 81-1 in a board of a requestor side returns the discernment bits Sa and Sb to "0" after the completion of sending out (Sa=1 ->0, Sb=1 ->0), and the address control section 81-1 in a board by the side of supply returns the discernment bits Sa and Sb to "0" after the completion of a transfer (refer to drawing 25 and drawing 26). (Sa=1 ->0, Sb=1 ->0) (processing C 1-10)
[0168] In case 256-bit data are transmitted to a 256-bit port, when a 128-bit band can be secured (in the

case of C2), a requestor-side and supply side performs the above-mentioned processing C 1-1 - C 1-3.
[0169] After that, the crossbar switch side address control section 61-1 by the side of supply answers Transfer O.K. to the address line of the side which recognizes and is vacant in seeing the discernment bits Sa and Sb and Port a or Port b using it, sets to "1" (Sa=0 ->1 or Sb=0 ->1) the discernment bits Sa and Sb which correspond simultaneously, and sends out a transfer request to a board (processing C 2-1).
[0170] The address control section 81-1 in a board by the side of supply directs to secure the path to a buffer group securable from the port secured to the switch control section 82-1 in a board. If Transfer O.K. is checked from one side of the two address lines, the crossbar switch side address control section 61-1 of a requestor side will set to "0" the discernment bits Sa and Sb of the direction to which Transfer O.K. did not come (0 1-> 1, 1->0, or 1), and will transmit Transfer O.K. to a board (processing C 2-2).
[0171] The address control section 81-1 in a board of a requestor side transmits Transfer O.K. to the controller 22-1 of equipment conventionally, and directs to make a switch (SW#2, SW#3) 75-1 and 76-1 the switch control section 82-1 in a board at a sending area (processing C 2-3).
[0172] The switch control section 82-1 in a board of a requestor side is c->a to the switch control section 82-1 in a board. or b, d->a or Routing of b is directed and new data are conventionally required once of two clocks at the output section of equipment. A transfer request is conventionally transmitted to the controller 22-1 of equipment, the switch control section 82-1 in a board switches switch (SW#11) 71a-1 or switch (SW#12) 71b-1 for every clock, and the address control section 81-1 in a board by the side of supply secures the path which sends data to the high order lower bit of a buffer group in order (processing C 2-4).
[0173] The switch control section 82-1 in a board of a requestor side sends out data, if directed setting out is performed. The switch control section 82-1 in a board by the side of supply receives the sent data by the buffer A group 77-1 or the buffer B group 78-1 (processing C 2-5). Henceforth, a requestor-side and supply side performs the above-mentioned processing C 1-8 - C 1-10 (refer to drawing 27 and drawing 28).
[0174] In case 256-bit data are transmitted to a 256-bit port, when a band cannot be secured (in the case of C3), a requestor-side and supply side performs the above-mentioned processing C 1-1 - C 1-3.
[0175] After that, the crossbar switch side address control section 61-1 by the side of supply recognizes that see the discernment bits Sa and Sb and Port a and Port b are using it, and answers a band secured improper signal (processing C 3-1).
[0176] The crossbar switch sidc address control section 61-1 of a requestor side transmits a band secured improper signal to a board as it is, and sets both the discernment bits Sa and Sb to "0" (processing C 3-2). (Sa=1 ->0, Sb=1 ->0)
[0177] The address control section 81-1 in a board of a requestor side transmits a band secured improper signal to the controller 22-1 of equipment as it is conventionally (processing C 3-3). Henceforth, he leaves it to the resending demand of the controller 22-1 of conventional equipment. When the cause of resending in equipment receipt-side is taking out conventionally, it is requiring even the controller 22-1 of the conventional equipment by the side of receipt, and is usable with the method (refer to drawing 29 and drawing 30).
[0178] In case 128-bit data are transmitted to a 256-bit port, when a 128-bit band can be secured (in the case of C4), the crossbar switch side address control section 61-1 of a requestor side sends out a transfer request to either of the two address lines by the side of receipt from the only address line. The crossbar switch side address control section 61-1 by the side of supply detects one transfer request of the two address lines (processing C 4-1).
[0179] The discernment bit of the side which checks that the crossbar switch side address control section 61-1 by the side of supply saw the discernment bits Sa and Sb, and Port a and either of the b are vacant as for it at least, and replies Transfer O.K. from the address line of vacant one of ports is set to "1" (processing C 4-2).
[0180] If Transfer O.K. is checked from one side of the two address lines, the crossbar switch side address control section 61-1 of a requestor side will transmit Transfer O.K. to a board, and will change the data receiver's address into a port with an answer henceforth. The address control section 81-1 in a

board transmits Transfer O.K. to the controller 22-1 of equipment as it is conventionally (processing C 4-3).

[0181] Then, in a supply side, the above-mentioned processing C 2-2 - C 2-5, and C 1-8 to 1-10 are performed. Moreover, in a requestor side, if processing C 4-3 is performed, the signal and data from a controller 22-1 of conventional equipment will be outputted as it is henceforth (refer to drawing 31 and drawing 32).

[0182] In case 128-bit data are transmitted to a 256-bit port, when a band cannot be secured (in the case of C5), the crossbar switch side address control section 61-1 of a requestor side sends out a transfer request to one address line of the receipt sides from the only address line. The crossbar switch side address control section 61-1 by the side of supply detects one transfer request of the two address lines (processing C 5-1).

[0183] The crossbar switch side address control section 61-1 by the side of supply recognizes that see the discernment bits Sa and Sb and Port a and Port b are using it, and answers a band secured improper signal (processing C 5-2).

[0184] The crossbar switch side address control section 61-1 of a requestor side transmits a band secured improper signal to a board as it is (processing C 5-3). Henceforth, he leaves it to the resending demand of the controller 22-1 of conventional equipment. When the cause of resending in equipment receipt-side is taking out conventionally, it is requiring even the controller 22-1 of the conventional equipment by the side of receipt, and is usable with the method (refer to drawing 33 and drawing 34).

[0185] In case 256-bit data are transmitted to a 128-bit port, when a 128-bit band can be secured (in the case of C6), the crossbar switch side address control section 61-1 of a requestor side sends out a transfer request to either of the two address lines. The crossbar switch side address control section 61-1 by the side of supply detects a transfer request from the address line (processing C 6-1).

[0186] The crossbar switch side address control section 61-1 by the side of supply replies Transfer O.K. to the address line in a sender's port. The crossbar switch side address control section 61-1 of a requestor side will transmit Transfer O.K. to a board, if Transfer O.K. is checked from the address line (processing C 6-2).

[0187] Then, in a requestor side, the above-mentioned processing C 2-3 - C 2-5, and C 1-8 to 1-10 are performed. Moreover, in a supply side, if processing C 6-2 is performed, a signal and data will be henceforth inputted into the controller 22-1 of conventional equipment conventionally as it is at equipment (refer to drawing 35 and drawing 36).

[0188] In case 256-bit data are transmitted to a 128-bit port, when a band cannot be secured (in the case of C7), the crossbar switch side address control section 61-1 of a requestor side sends out a transfer request from either of the two address lines. The crossbar switch side address control section 61-1 by the side of supply detects a transfer request from the address line (processing C 7-1).

[0189] The crossbar switch side address control section 61-1 by the side of supply replies a band secured improper signal to the address line with a sender's port. The crossbar switch side address control section 61-1 of a requestor side will transmit a band secured improper signal to a board, if a band secured improper signal is checked from the address line (processing C 7-2).

[0190] Henceforth, he leaves it to the resending demand of the controller 22-1 of conventional equipment. When the cause of resending in equipment receipt-side is taking out conventionally, it is requiring even the controller 22-1 of the conventional equipment by the side of receipt, and is usable with the method (refer to drawing 37 and drawing 38).

[0191] Thus, since it has the switch and controller which distribute data to two input buffers and this in the board which can receive data with wide width of face, it can transmit to the board and coincidence from which two data width of face differs.

[0192] Moreover, since it has the switch and controller which distribute data to the point of the output buffer of the board which can send data with wide width of face, if the port equivalent to half data width of face is intact even if data are under transfer, another data transfer can be performed.

[0193] Furthermore, since the address line, a 2 bits discernment bit, and one 1-bit a and b port discernment line are used instead of preparing 2 sets of address lines, physical size for a connection can

be made small and it can realize cheaply.
[0194] Since common use-ization is in drawing further again, without the data line/address line being dependent on the bus width of face of a communications partner, it is cheaply realizable rather than it prepares two or more ports doubled with the data width of face of a communications partner.
[0195]
[Effect of the Invention] As explained above, according to this invention, it has two or more ports of the same data width of face where two or more boards are connected, respectively. In the data width-of-face adjustable mold crossbar switch equipment which connects between two or more boards through two or more ports which share an address signal By performing the communication link with other boards through the port which has **ed of the ports where a board with wide data width of face is connected, in case the data width of face of the boards which communicate differs It is effective in the ability for the data width of face connected to the crossbar switch not to be concerned, and communicate to the data width of face of a phase hand's port in a large port, also during the communication link with the port where data width of face is narrow.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the configuration of the crossbar switch equipment by one example of this invention.
[Drawing 2] It is the block diagram showing the configuration of the crossbar switch side I/O section of drawing 1 .
[Drawing 3] It is the block diagram showing the configuration of the data division of drawing 1 .
[Drawing 4] It is the block diagram showing the configuration of the address control section of drawing 1 .
[Drawing 5] It is the block diagram showing the configuration of the switch in a board of drawing 3 .
[Drawing 6] (a) and (b) are drawings showing the configuration of the switch shown in drawing 3 and drawing 5 .
[Drawing 7] It is the block diagram showing the configuration of a crossbar switch side address control section shown in drawing 2 .
[Drawing 8] Drawing in which (a) shows the content of storage of the memory (A) of drawing 7 , and (b) are drawings showing the content of storage of the memory (B) of drawing 7 .
[Drawing 9] It is the block diagram showing the configuration of the address control section in a board of drawing 4 .
[Drawing 10] Drawing in which (a) shows the content of storage of the memory (C) of drawing 9 , and (b) are drawings showing the content of storage of the memory (D) of drawing 9 .
[Drawing 11] It is drawing showing control of the switch of drawing 3 by the switch control section in a board of drawing 4 , and drawing 5 .
[Drawing 12] It is the flow chart which shows the actuation of a crossbar switch side address control section shown in drawing 2 and drawing 7 .
[Drawing 13] It is the flow chart which shows the actuation of a crossbar switch side address control section shown in drawing 2 and drawing 7 .
[Drawing 14] It is the flow chart which shows the actuation of a crossbar switch side address control section shown in drawing 2 and drawing 7 .
[Drawing 15] It is the flow chart which shows the actuation of a crossbar switch side address control section shown in drawing 2 and drawing 7 .
[Drawing 16] It is the flow chart which shows the actuation of the address control section in a board shown in drawing 4 and drawing 9 .
[Drawing 17] It is the flow chart which shows the actuation of the address control section in a board shown in drawing 4 and drawing 9 .
[Drawing 18] It is the flow chart which shows the actuation of the address control section in a board shown in drawing 4 and drawing 9 .
[Drawing 19] It is the flow chart which shows the actuation of the address control section in a board shown in drawing 4 and drawing 9 .
[Drawing 20] It is the flow chart which shows the actuation of the address control section in a board

shown in drawing 4 and drawing 9 .
[Drawing 21] It is the flow chart which shows the actuation of the address control section in a board shown in drawing 4 and drawing 9 .
[Drawing 22] It is the flow chart which shows the actuation of the address control section in a board shown in drawing 4 and drawing 9 .
[Drawing 23] It is the flow chart which shows the actuation of the address control section in a board shown in drawing 4 and drawing 9 .
[Drawing 24] It is drawing in which showing a division in the case of the data transfer in the crossbar switch equipment by one example of this invention.
[Drawing 25] In case the 256-bit data based on one example of this invention are transmitted to a 256-bit port, it is drawing showing actuation of a requestor side when a 256-bit band is securable.
[Drawing 26] In case the 256-bit data based on one example of this invention are transmitted to a 256-bit port, it is drawing showing the actuation by the side of supply when a 256-bit band is securable.
[Drawing 27] In case the 256-bit data based on one example of this invention are transmitted to a 256-bit port, it is drawing showing actuation of a requestor side when a 128-bit band is securable.
[Drawing 28] In case the 256-bit data based on one example of this invention are transmitted to a 256-bit port, it is drawing showing the actuation by the side of supply when a 128-bit band is securable.
[Drawing 29] In case the 256-bit data based on one example of this invention are transmitted to a 256-bit port, it is drawing showing actuation of a requestor side when a band is not securable.
[Drawing 30] In case the 256-bit data based on one example of this invention are transmitted to a 256-bit port, it is drawing showing the actuation by the side of supply when a band is not securable.
[Drawing 31] In case the 128-bit data based on one example of this invention are transmitted to a 256-bit port, it is drawing showing actuation of a requestor side when a 128-bit band is securable.
[Drawing 32] In case the 128-bit data based on one example of this invention are transmitted to a 256-bit port, it is drawing showing the actuation by the side of supply when a 128-bit band is securable.
[Drawing 33] In case the 128-bit data based on one example of this invention are transmitted to a 256-bit port, it is drawing showing actuation of a requestor side when a band is not securable.
[Drawing 34] In case the 128-bit data based on one example of this invention are transmitted to a 256-bit port, it is drawing showing the actuation by the side of supply when a band is not securable.
[Drawing 35] In case the 256-bit data based on one example of this invention are transmitted to a 128-bit port, it is drawing showing actuation of a requestor side when a 128-bit band is securable.
[Drawing 36] In case the 256-bit data based on one example of this invention are transmitted to a 128-bit port, it is drawing showing the actuation by the side of supply when a 128-bit band is securable.
[Drawing 37] In case the 256-bit data based on one example of this invention are transmitted to a 128-bit port, it is drawing showing actuation of a requestor side when a band is not securable.
[Drawing 38] In case the 256-bit data based on one example of this invention are transmitted to a 128-bit port, it is drawing showing the actuation by the side of supply when a band is not securable.
[Drawing 39] It is the block diagram showing the configuration of the crossbar switch equipment by the conventional example.
[Drawing 40] It is the block diagram showing the configuration of the processor board of drawing 39 .
[Description of Notations]
1 Crossbar Switch Equipment
2-1, 2-2 Processor board
3-1, 3-2 Memory board
4-1 to 4-4 I/O board
5 Crossbar Switch
6-1 to 6-4 Crossbar switch side I/O section
7-1 to 7-4 Data division
8-1 to 8-4 Address control section
61-1 It is Address <Control-Section BR> 61a-1 Crossbar Switch Side. Controller
61b-1 Memory (A)

61c-1 Memory (B)
71-1 Switch in Board
72-1, 73-1 Buffer
74-1 to 76-1,
71a-1-71j-1 Switch
77-1 Buffer A Group
78-1 Buffer B Group
81-1 Address Control Section in Board
81a-1 Controller
81b-1 Memory (C)
81c-1 Memory (D)
81d-1-81g-1 Counter
82-1 Switch Control Section in Board

[Translation done.]